

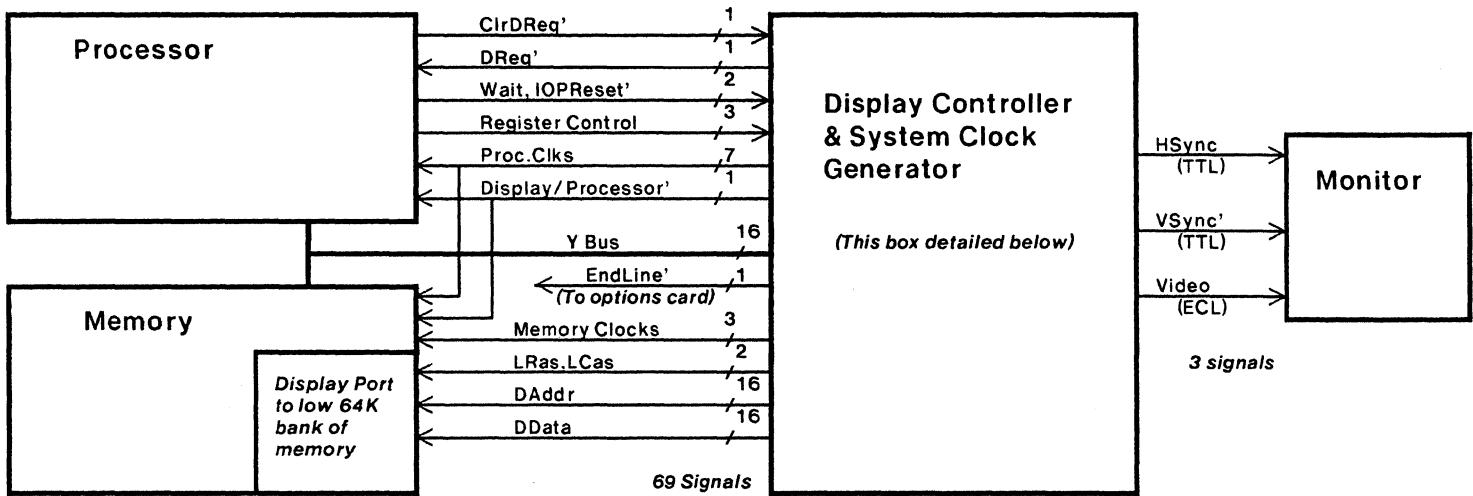
TABLE OF CONTENTS

SHEET

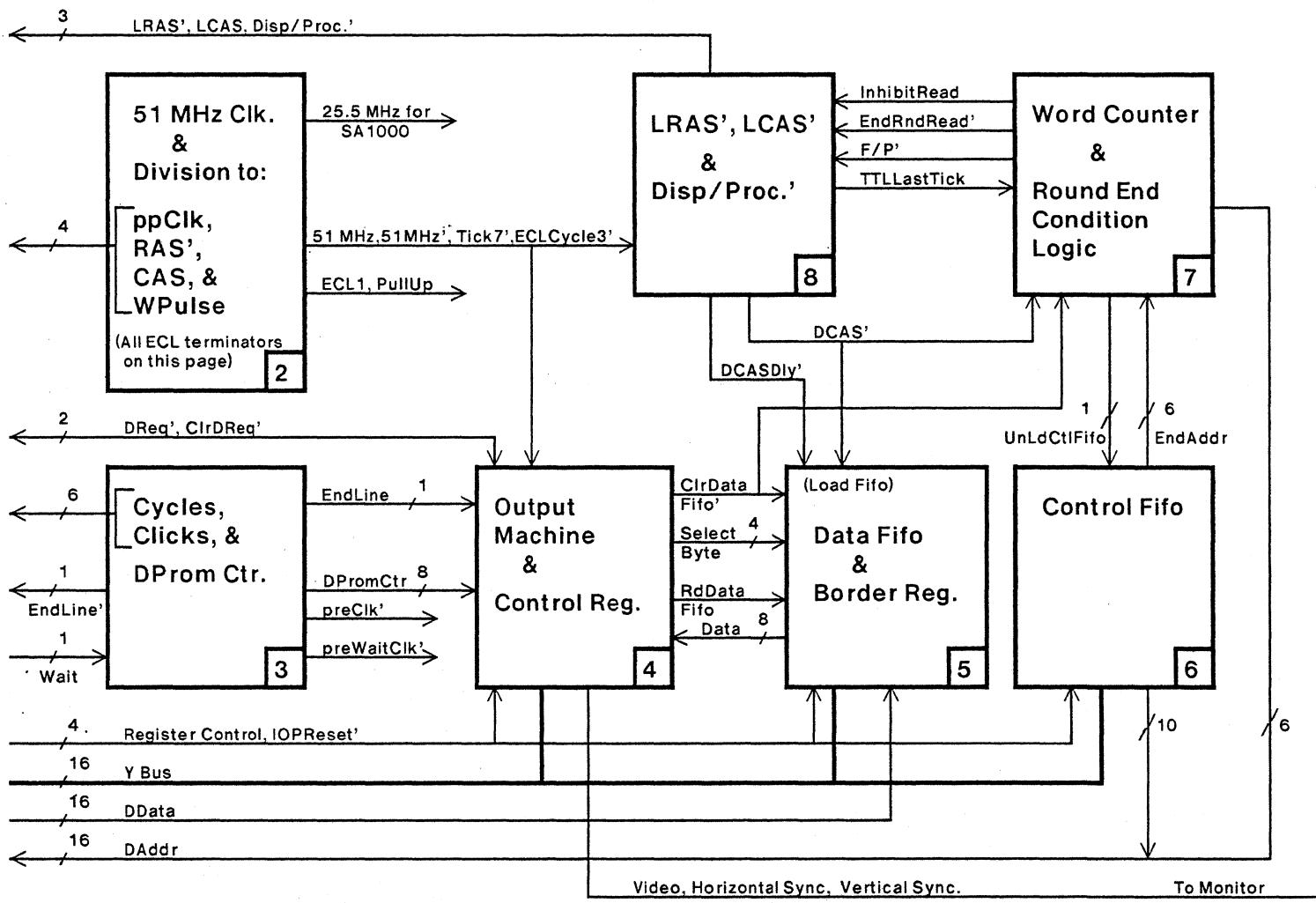
0.40	BLOCK DIAGRAM: DISPLAY AND CLOCK LOGIC
0.41	BLOCK DIAGRAM: SYSTEM CLOCK GENERATION
0.42	BLOCK DIAGRAM: DISK CONTROLLER OVERVIEW
0.43	BLOCK DIAGRAM: PROCESSOR INTERFACE
0.44	BLOCK DIAGRAM: SERIALIZER/DESERIALIZER
0.45	BLOCK DIAGRAM: OUTPUT CONDITIONING CIRCUITS
0.46	BLOCK DIAGRAM: INPUT CONDITIONING CIRCUITS
1	POWER SUPPLY AND FUSES
2	51 MHZ CLOCK DIVIDERS
3	CYCLES, CLICKS, AND DISPLAY COUNTER
4	DISPLAY OUTPUT MACHINE AND CONTROL REGISTER
5	DATA FIFO AND BORDER REGISTER
6	CONTROL FIFO DATA PATH
7	READ MACHINE: WORK COUNTER & END CONDITIONS
8	LCAS & LRAS' GENERATION
9	DISCRETES & CONNECTORS
10	TESTABILITY SIGNALS
11	ECL TERMINATORS
12	CONTROL AND WRITE DATA REGISTERS
13	STATUS/TEST MUX, READ DATA REGISTER
14	SERVICE REQUEST, OVER RUN, & WORD STATUS BUFFER
15	SERIALIZER/DESERIALIZER
16	FIELD & WORD STATE MACHINE
17	MFM ENCODING, PRE-COMPENSATION & ADDRESS MARK GENERATION
18	DISK OUTPUT BUFFERS AND DRIVERS
19	PHASE DECODER LOGIC
20	DISK INPUT BUFFERS AND RECEIVERS
21	MISCELLANEOUS INPUT CLOCKS AND MULTIPLEXING
22	DATA SEPARATOR AND ADDRESS MARK DETECTION
23	INPUT MULTIPLEXOR
24	DISK CABLES AND DISCRETES
25	PHASE DECODER OSCILLATOR
26	DISCRETE PHASE COMPARATOR
27	TESTABILITY SIGNALS
28	FILTER CAPACITORS
29	TEST POINT LISTING, EDGE CONNECTOR LISTING, & SIGNAL LISTING

HSIO-0.3B.SIL

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS		DWG SIZE A4	DWG NO. 156P11448		SHEET REV. B
	TITLE SCHEMATIC, HSIO			SHEET 0.3 OF		

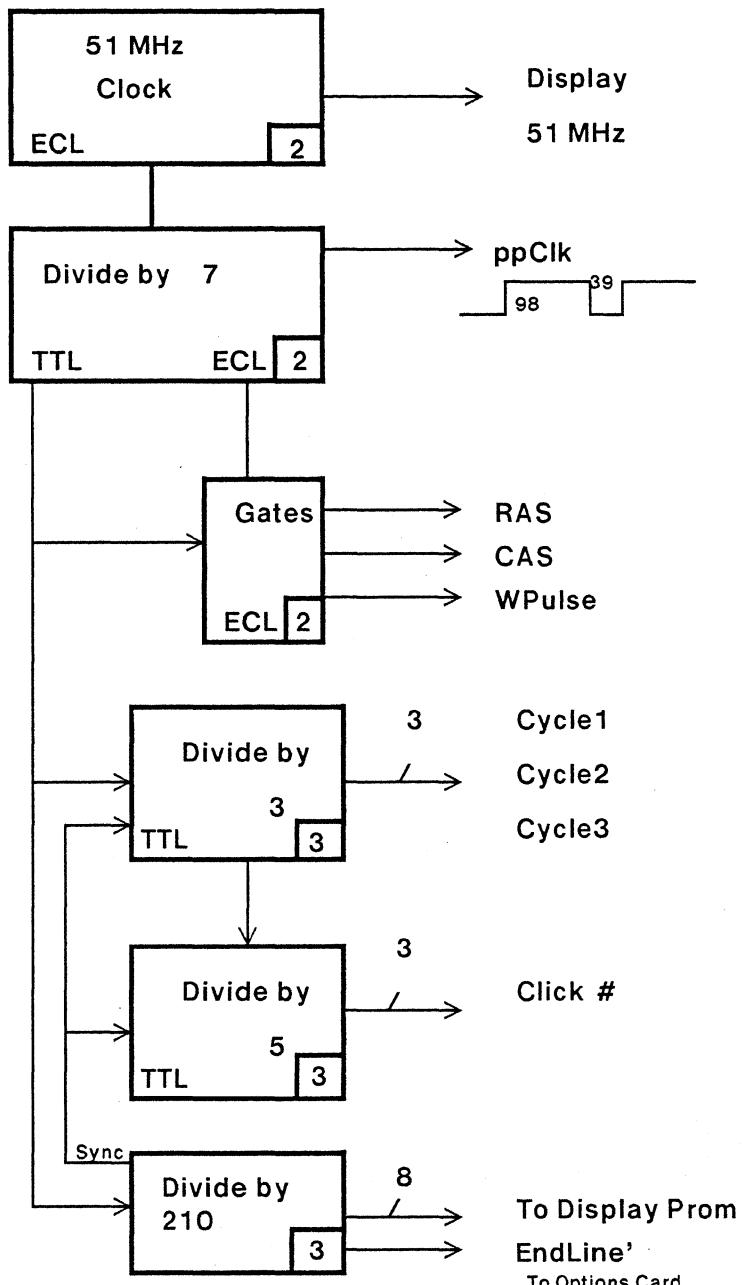


Relationship and Interconnection of Display & Clocks to rest of Dandelion



Detail Block Diagram of Display & Clocks

(Logic drawing page number is in lower right corner of each box.)



Timing

$$1470 = 7 * 2 * 5 * 3 * 7$$

1470 Bit times/line

210 clicks/line

14 Rounds/Line

5 clicks/round

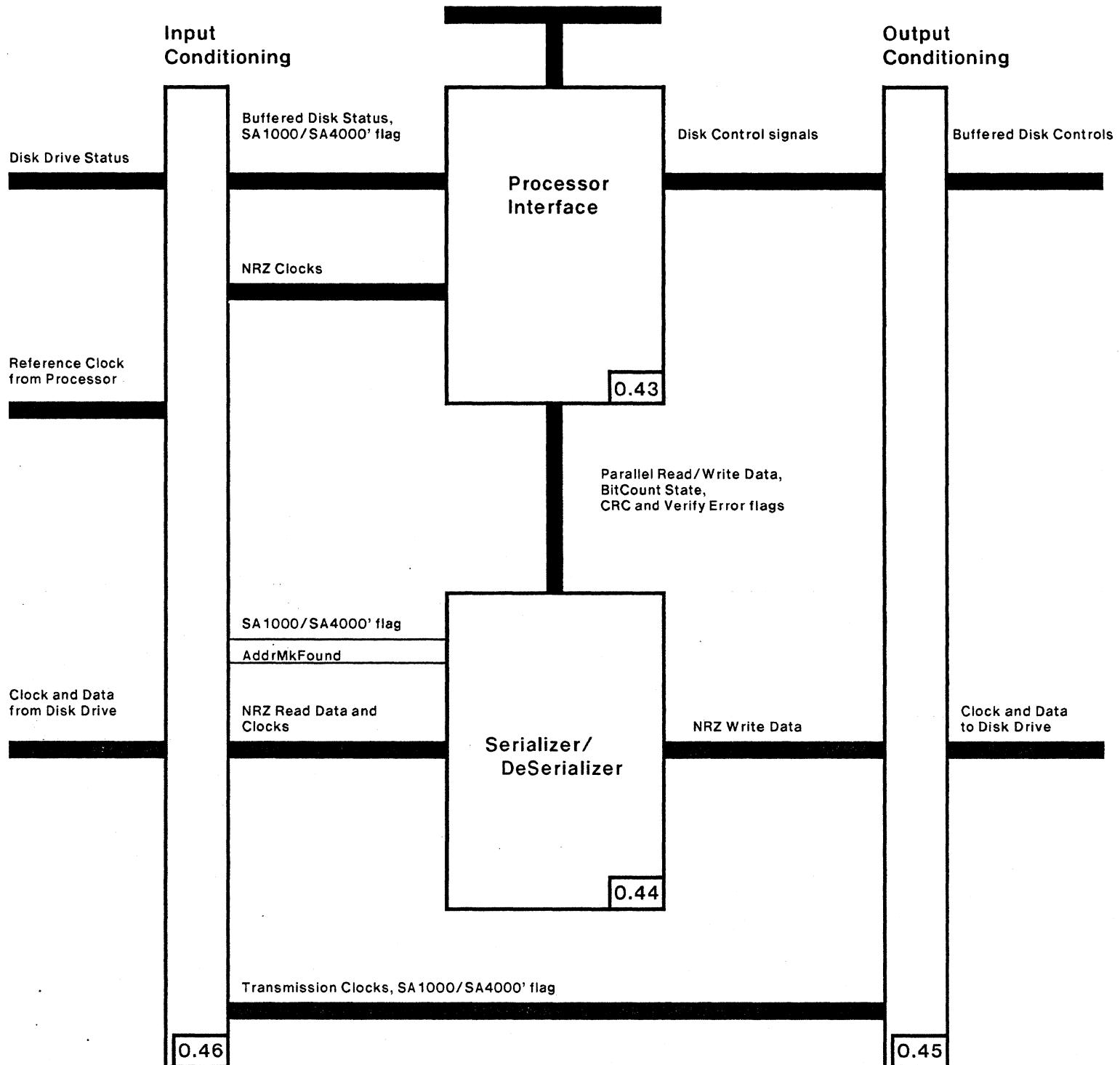
3 cycles/click

7 display bit times/cycle

SYSTEM CLOCK GENERATION BLOCK DIAGRAM

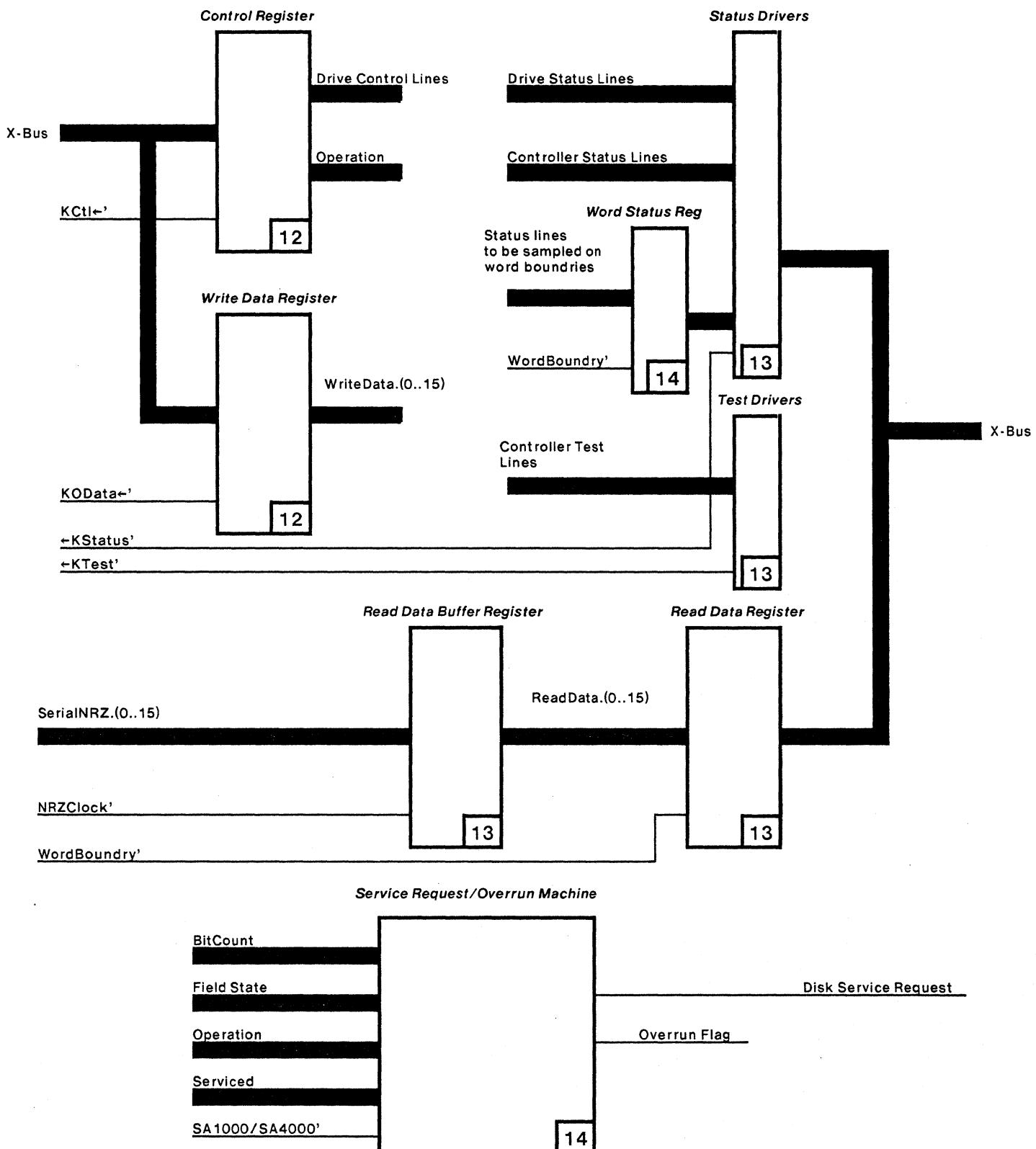
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11448	SHEET REV.
	TITLE SCHEMATIC, HSIO	A4	SHEET 0.41 OF	B

X Bus, Control Signals



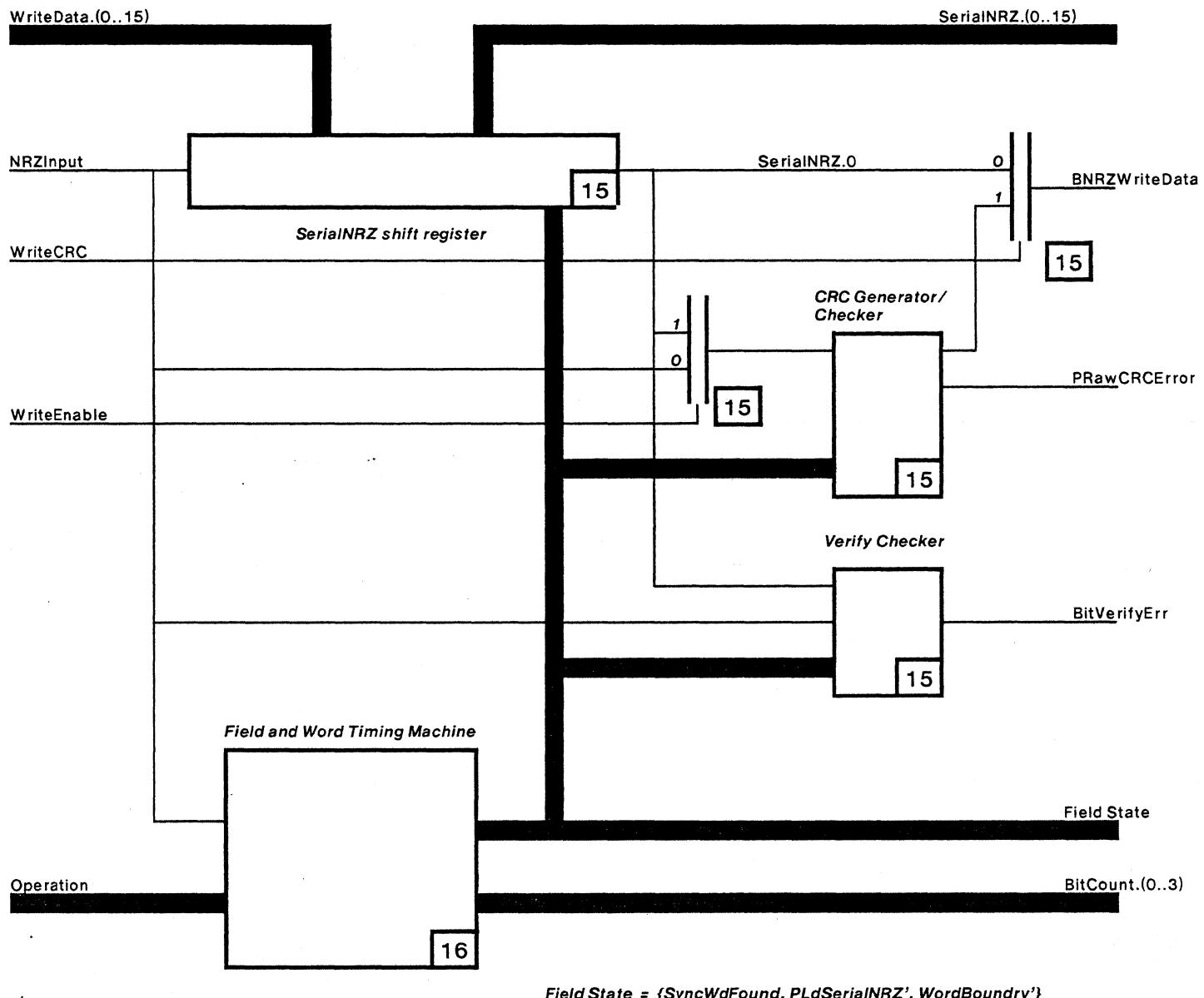
DISK CONTROLLER BLOCK DIAGRAM

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11448	SHEET REV. B
	TITLE SCHEMATIC, HSIO			



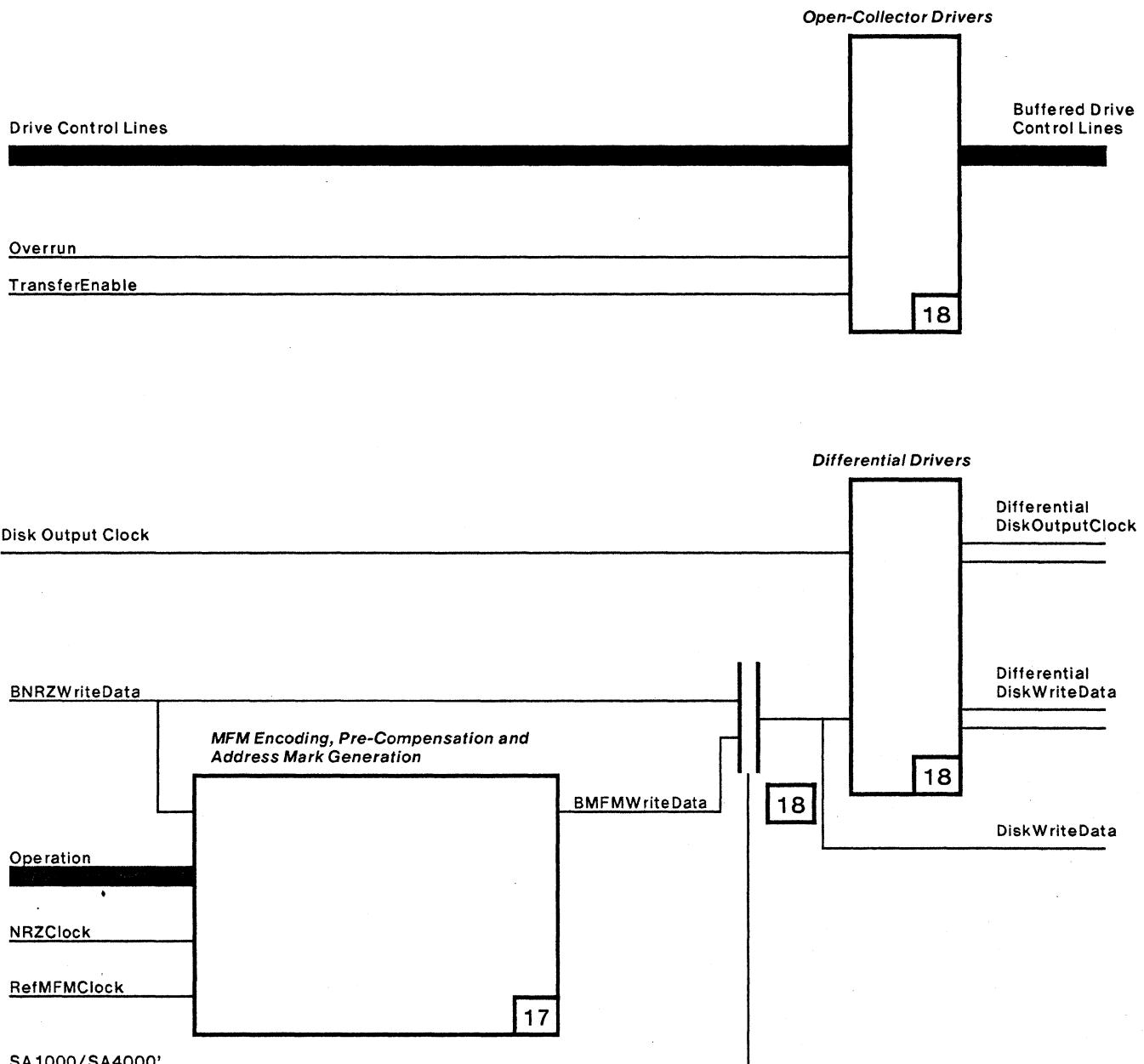
PROCESSOR INTERFACE BLOCK DIAGRAM

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO.	156P11448	SHEET REV.
	TITLE SCHEMATIC, HSIO				



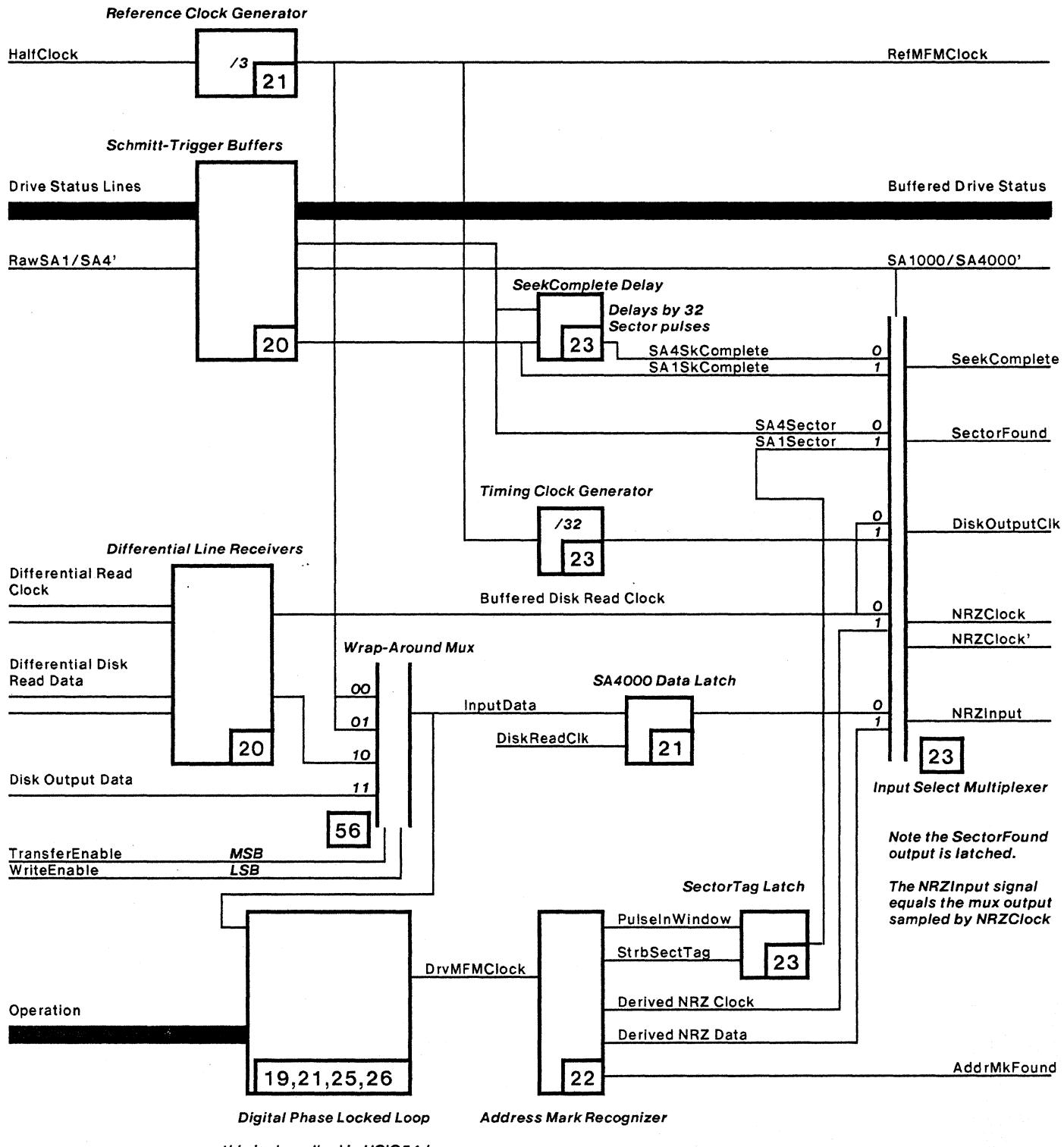
SERIALIZER/DESERIALIZER BLOCK DIAGRAM

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG	DWG NO. 156P11448	SHEET
		SIZE A4	0.44 OF	REV. B
TITLE	SCHEMATIC, HSIO			



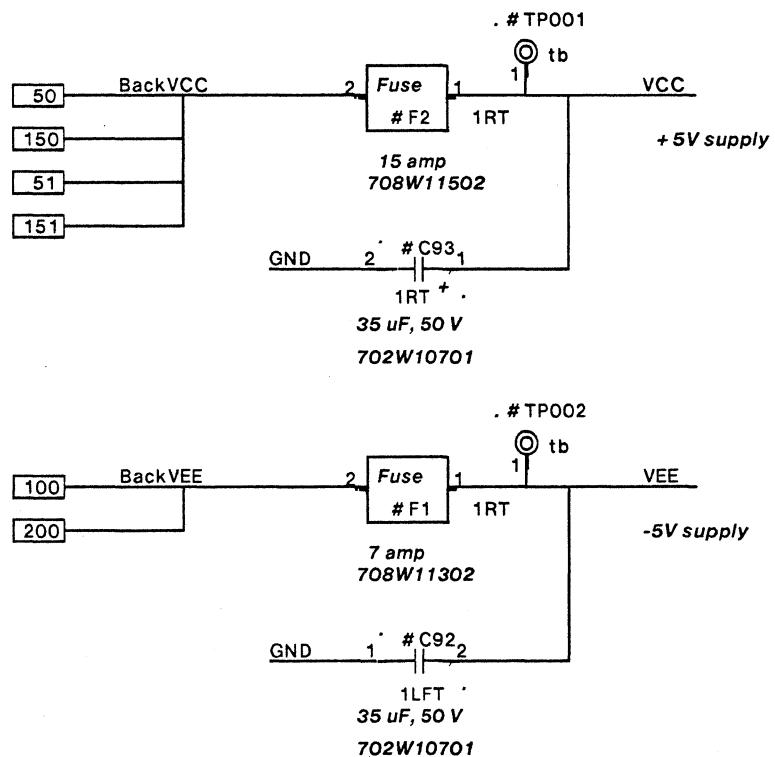
OUTPUT CONDITIONING CIRCUITS BLOCK DIAGRAM

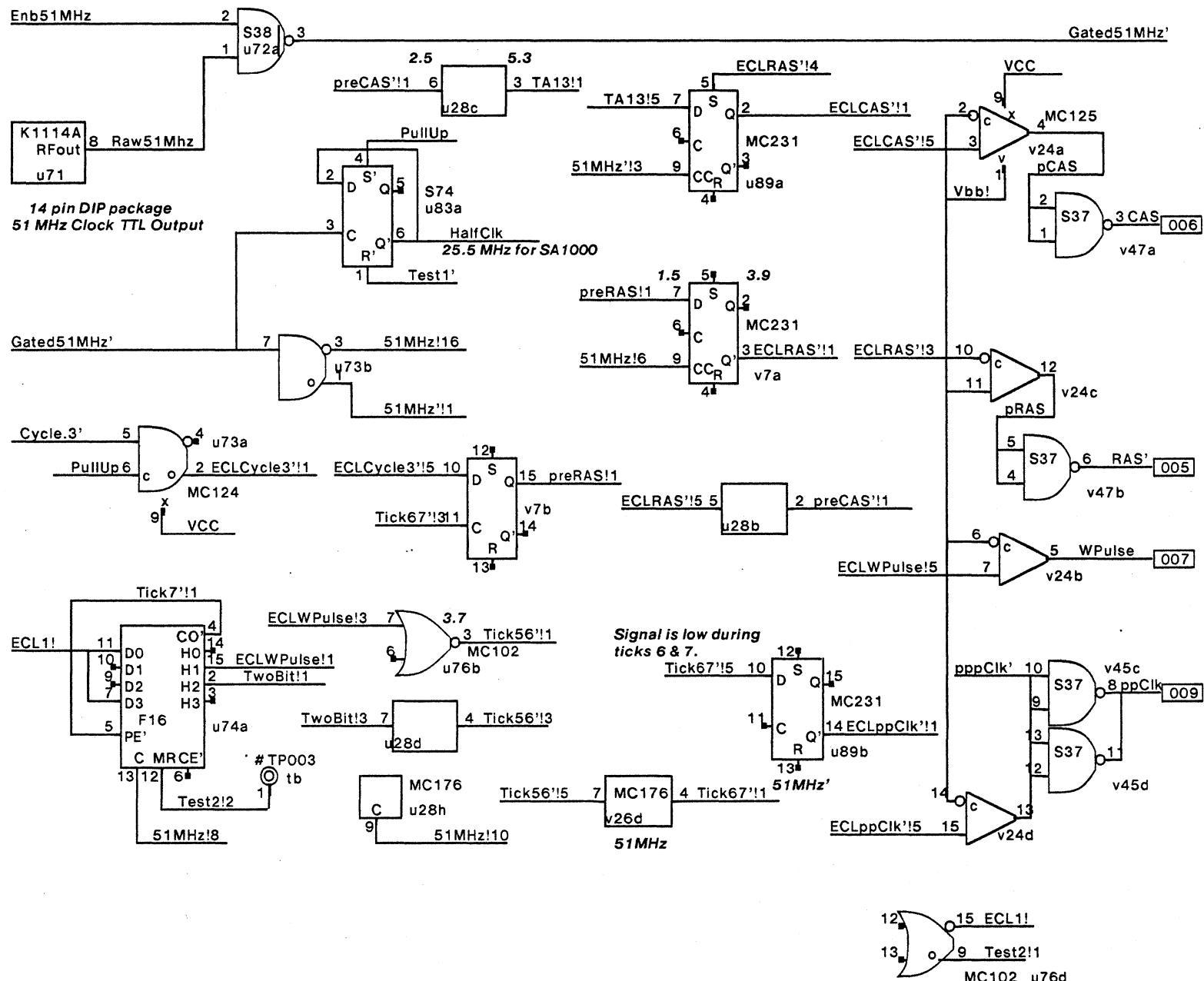
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE A4	DWG NO. 156P11448	SHEET REV. B
	TITLE SCHEMATIC, HSIO			



INPUT CONDITIONING CIRCUITS BLOCK DIAGRAM

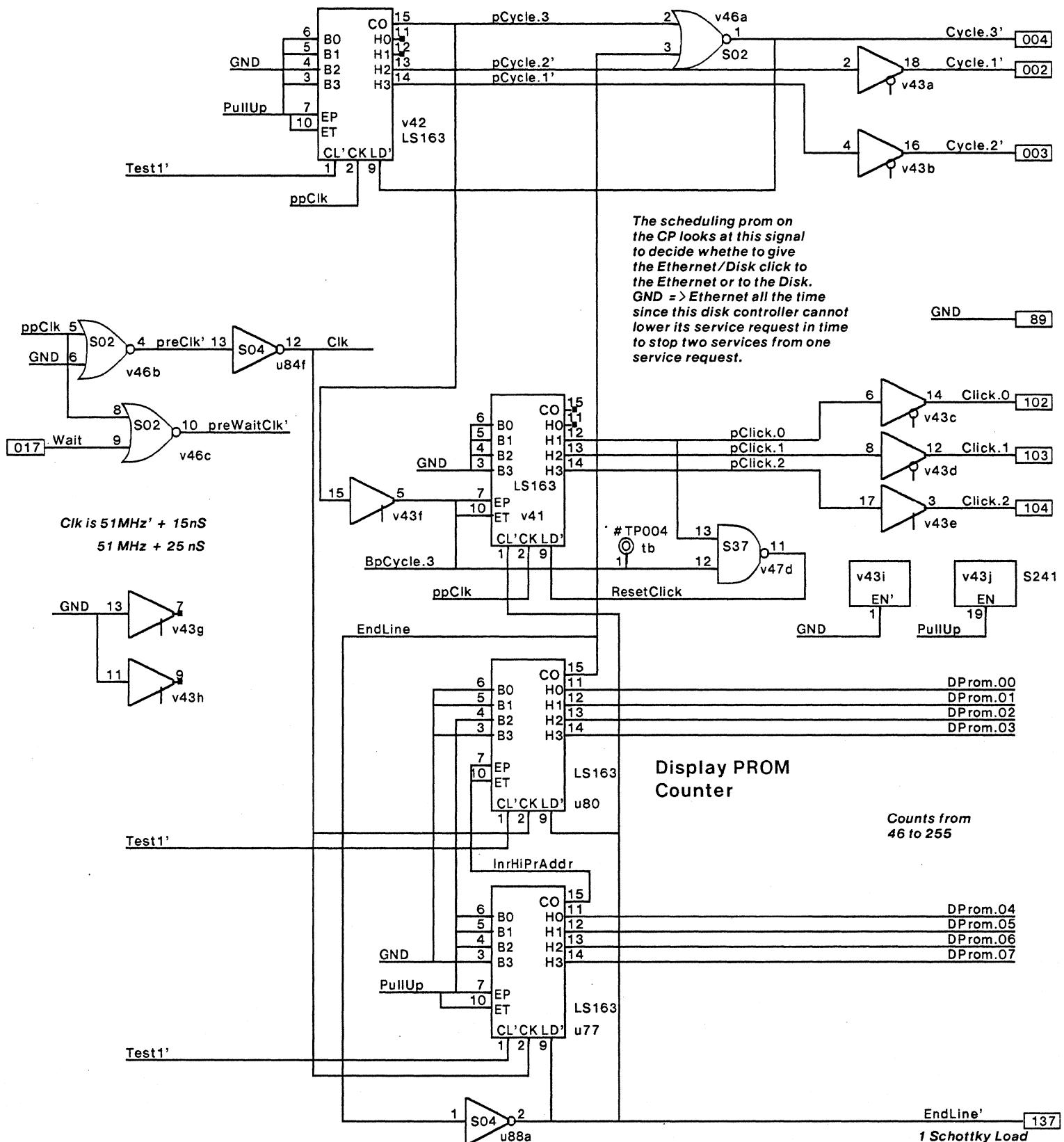
XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11448	SHEET REV.
	TITLE SCHEMATIC, HSIO	A4	SHEET 0.46 OF	B

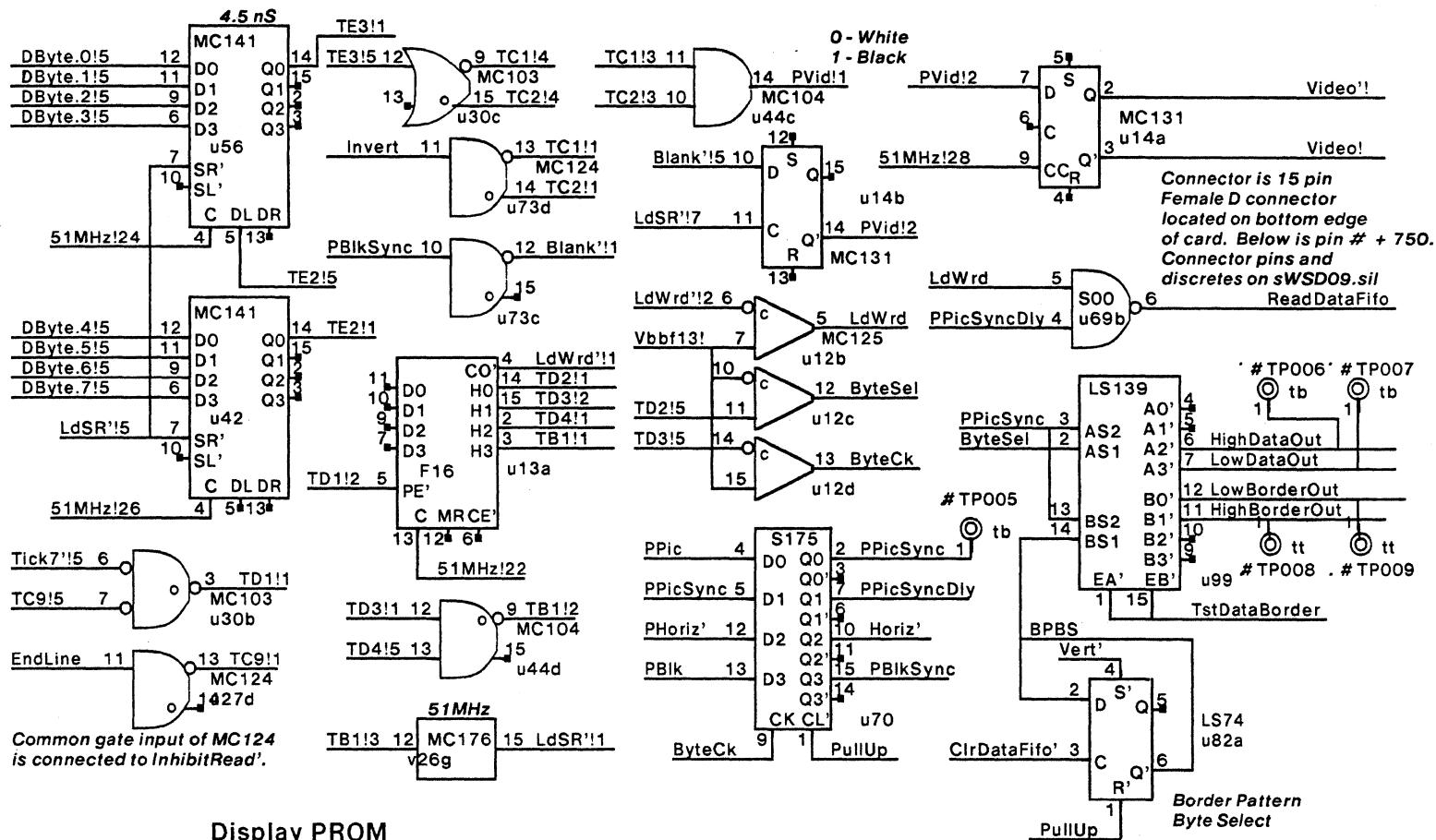




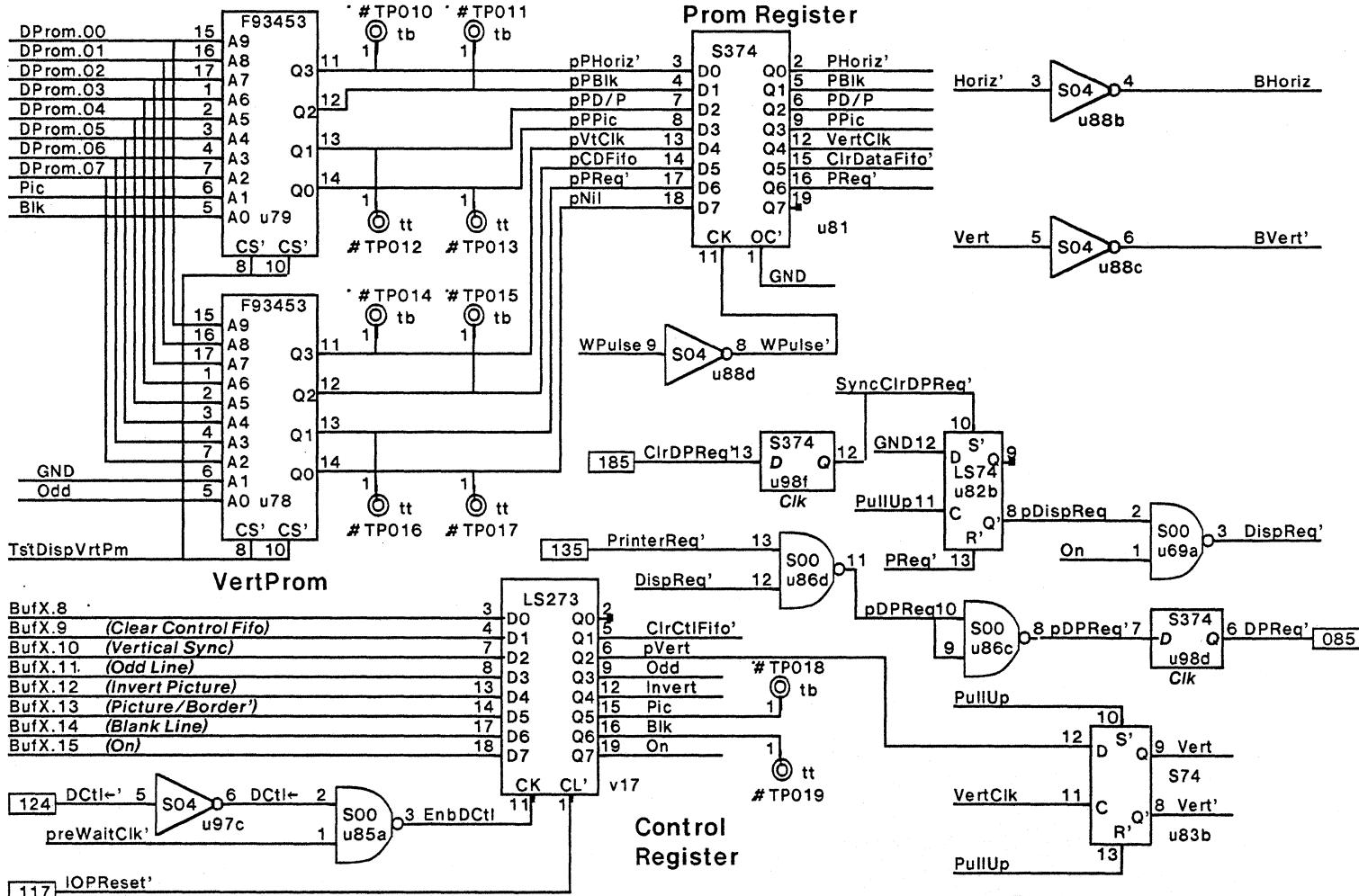
Note: The prefix **#%** in front of chip position causes the chip to be wired upside down in socket. This prevents cutting of ground connections on stitchweld card. The suffix **!** prevents Route from attempting automatic terminator assignment since D0 stitchweld card has none defined. Subnet wiring order for a net is done by appending to the net name a **!** followed by the wiring sequence number of the node in the net. Automatic terminator assignment is inhibited by use of **!** as the last character in the character string of the net. This must occur after the subnet feature if it is also being used.

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11448	SHEET REV.
	TITLE SCHEMATIC, HS10	A4	02 OF	B

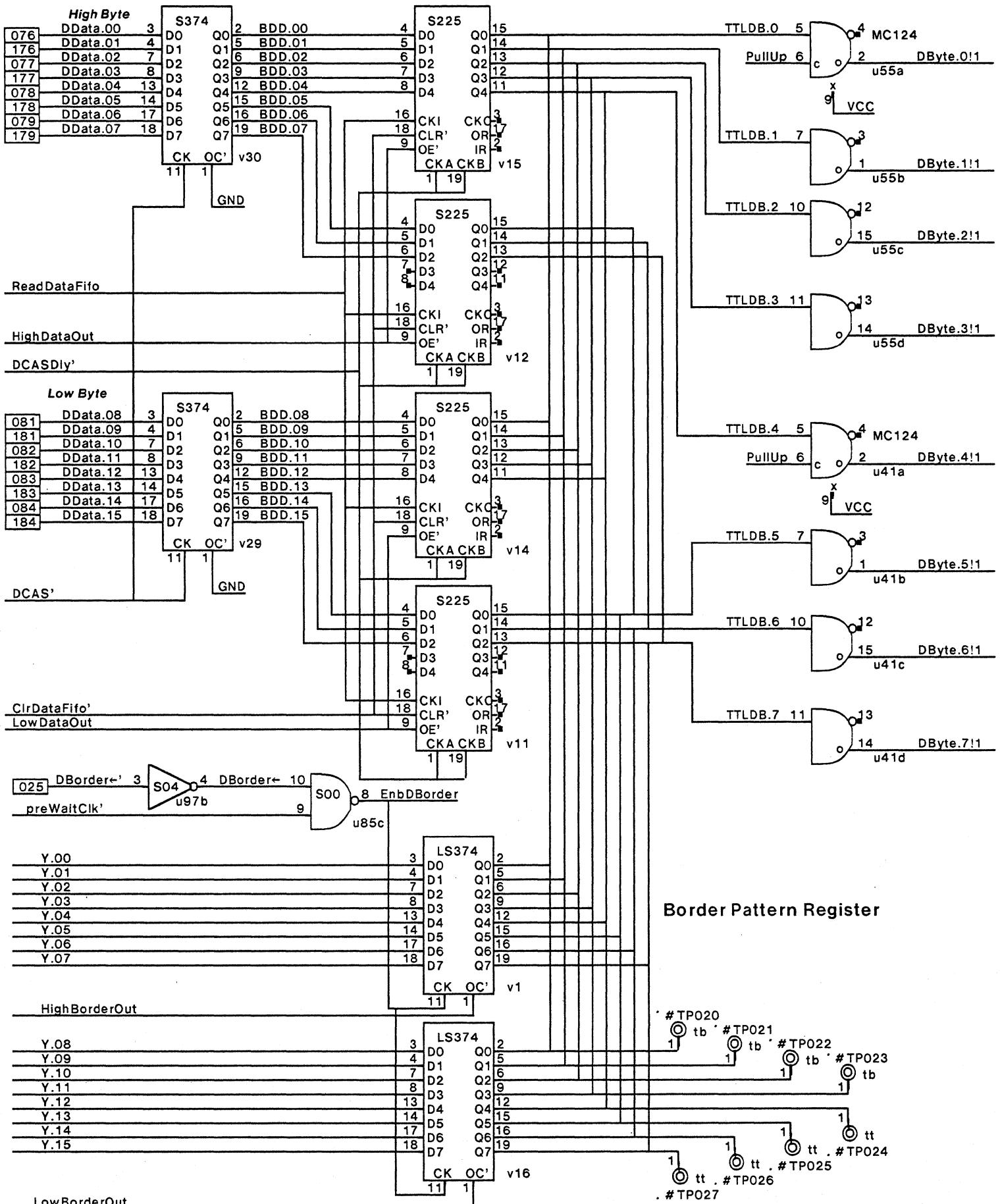




Display PROM



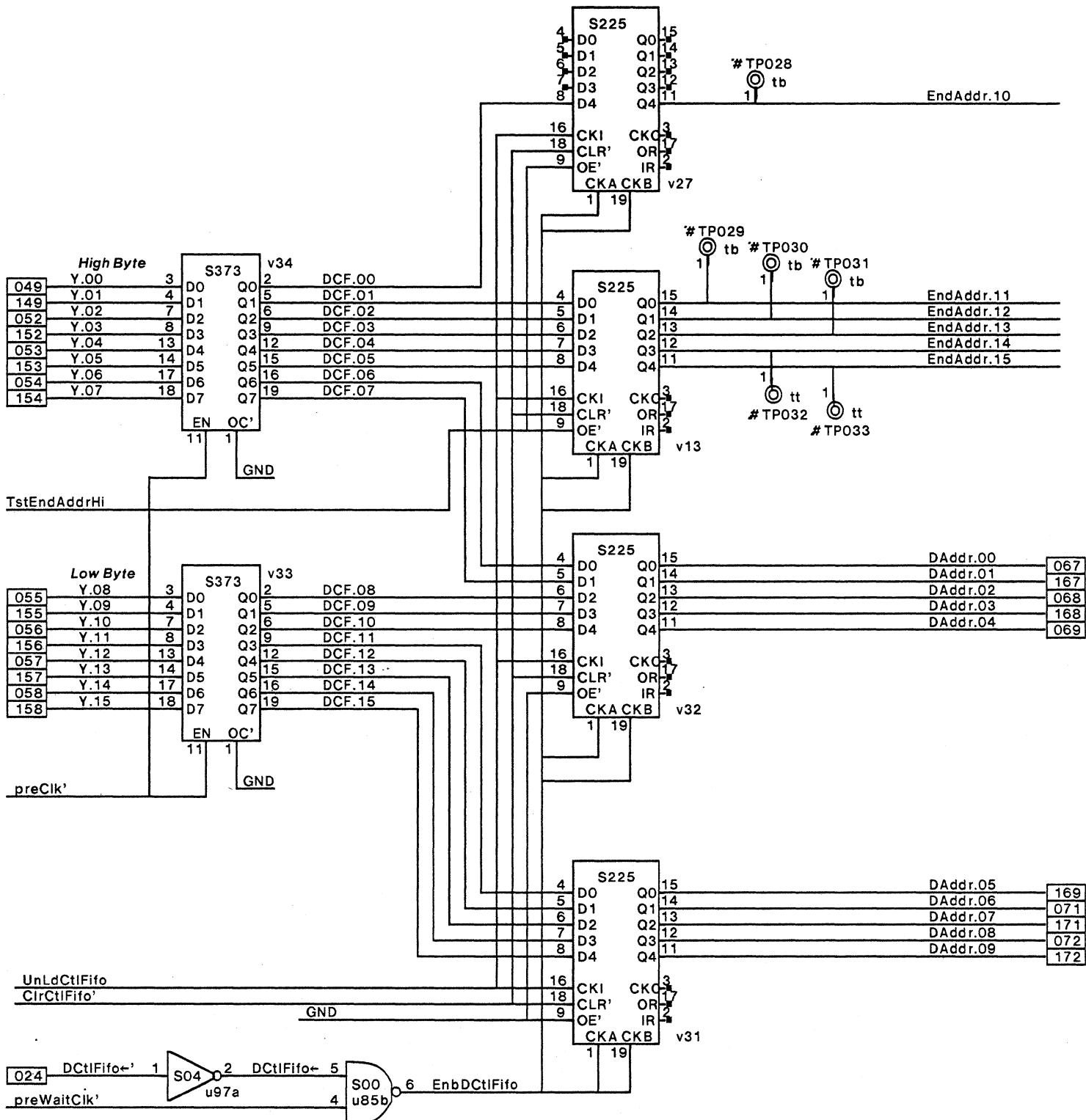
Terminators shown on clock page.

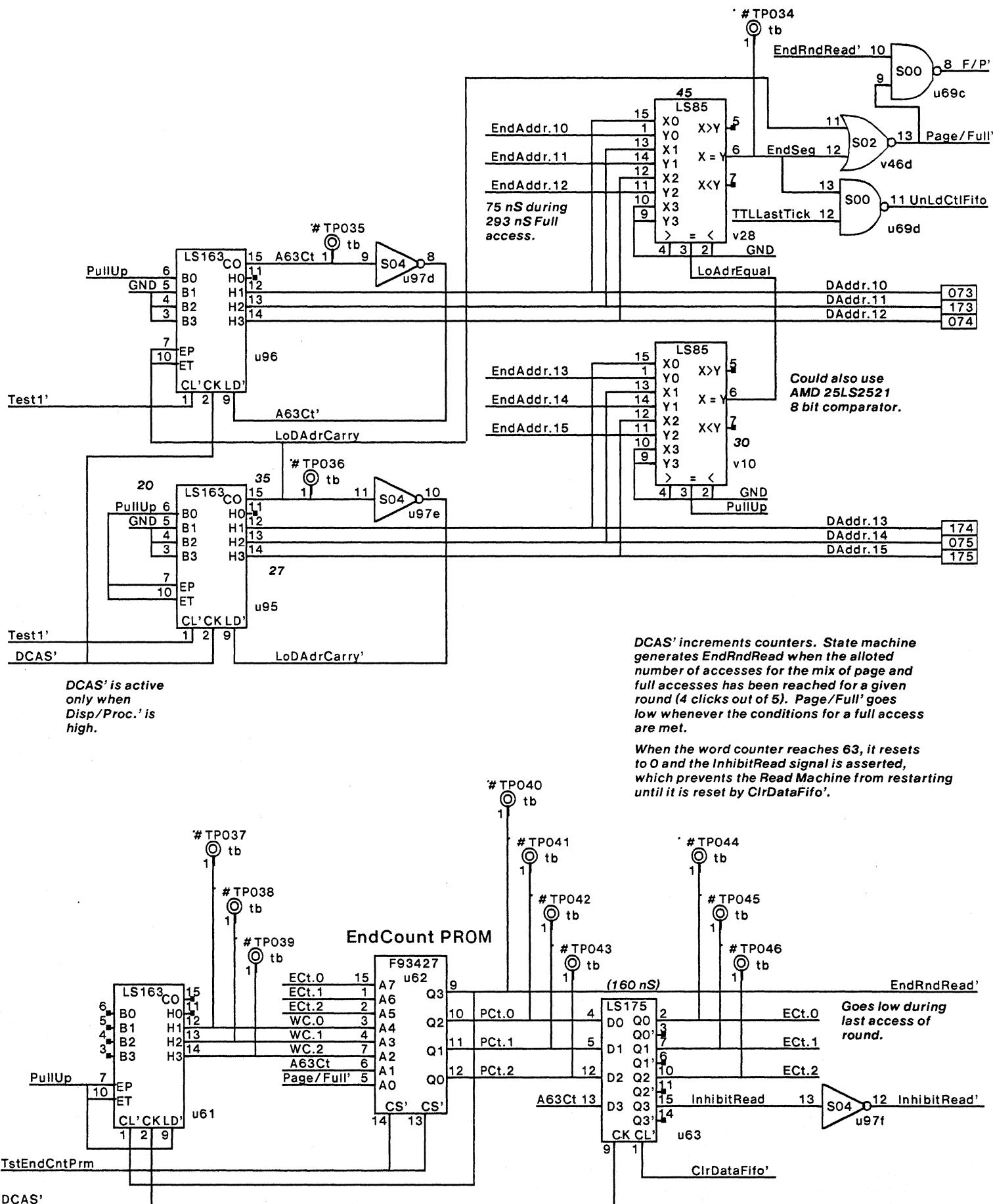


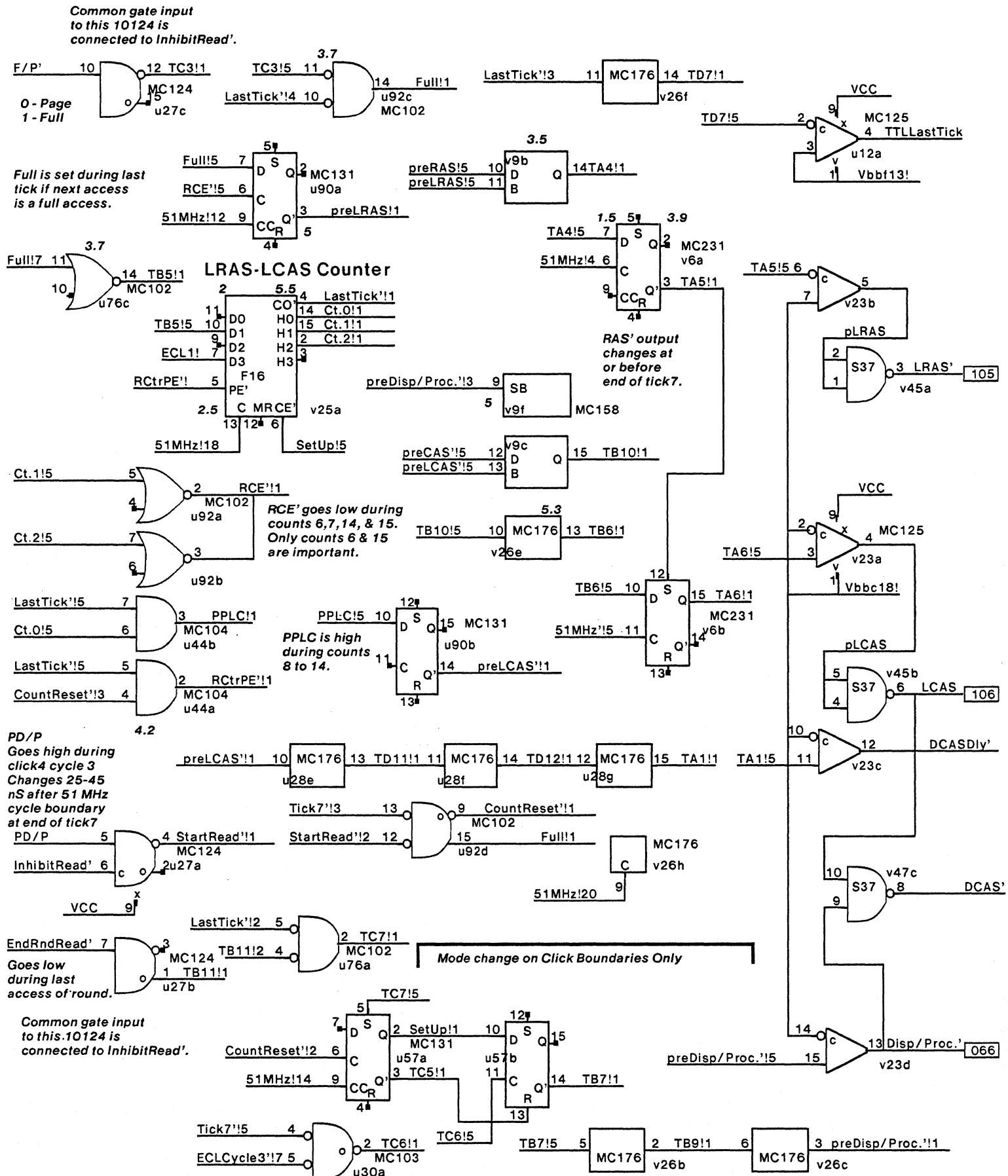
EndLine goes low once per horizontal line.

DCASDly' is DCAS' delayed by 20 nS.

Read signal goes low for 20 nS before low data byte is latched by the shift register.

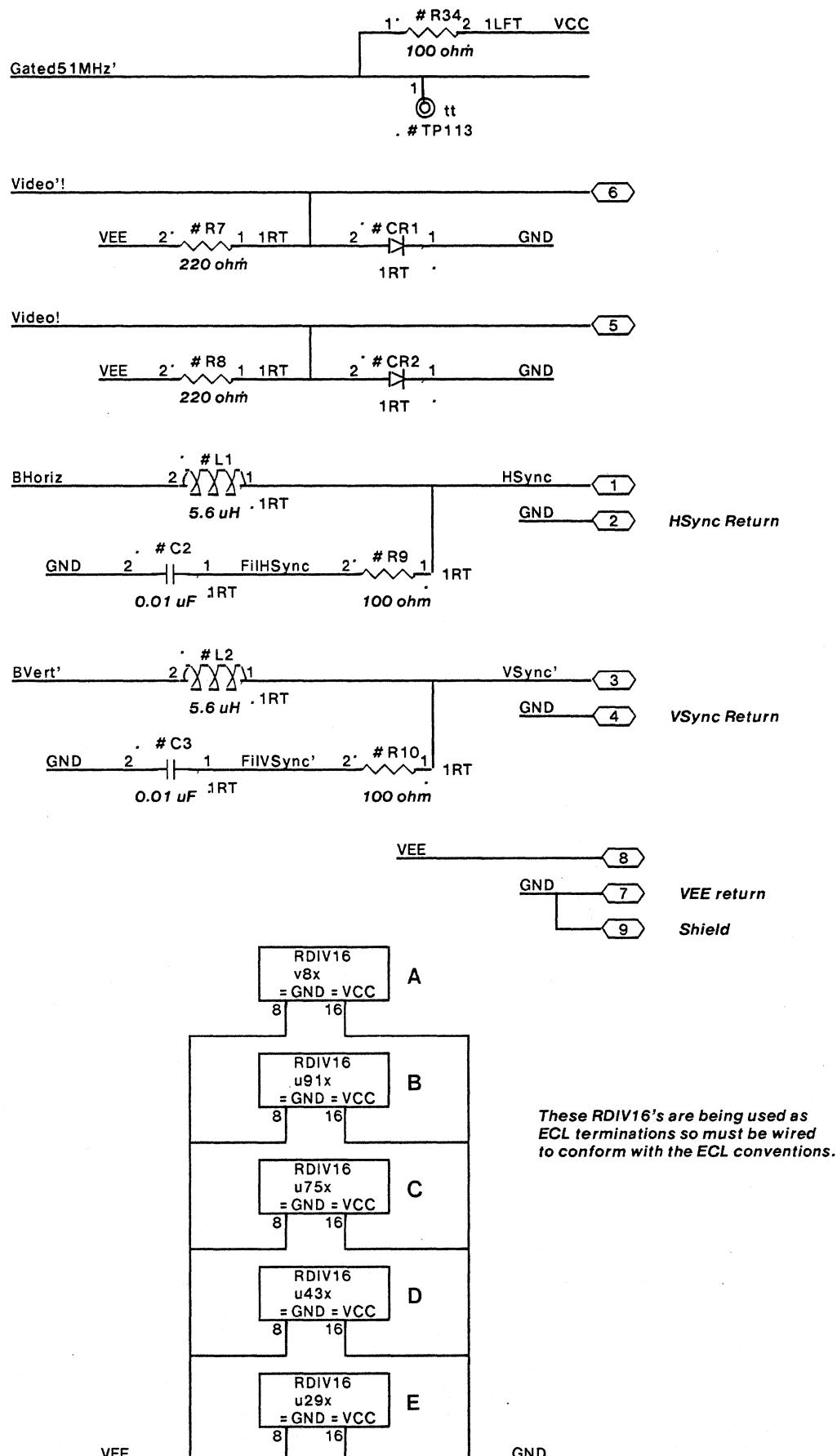




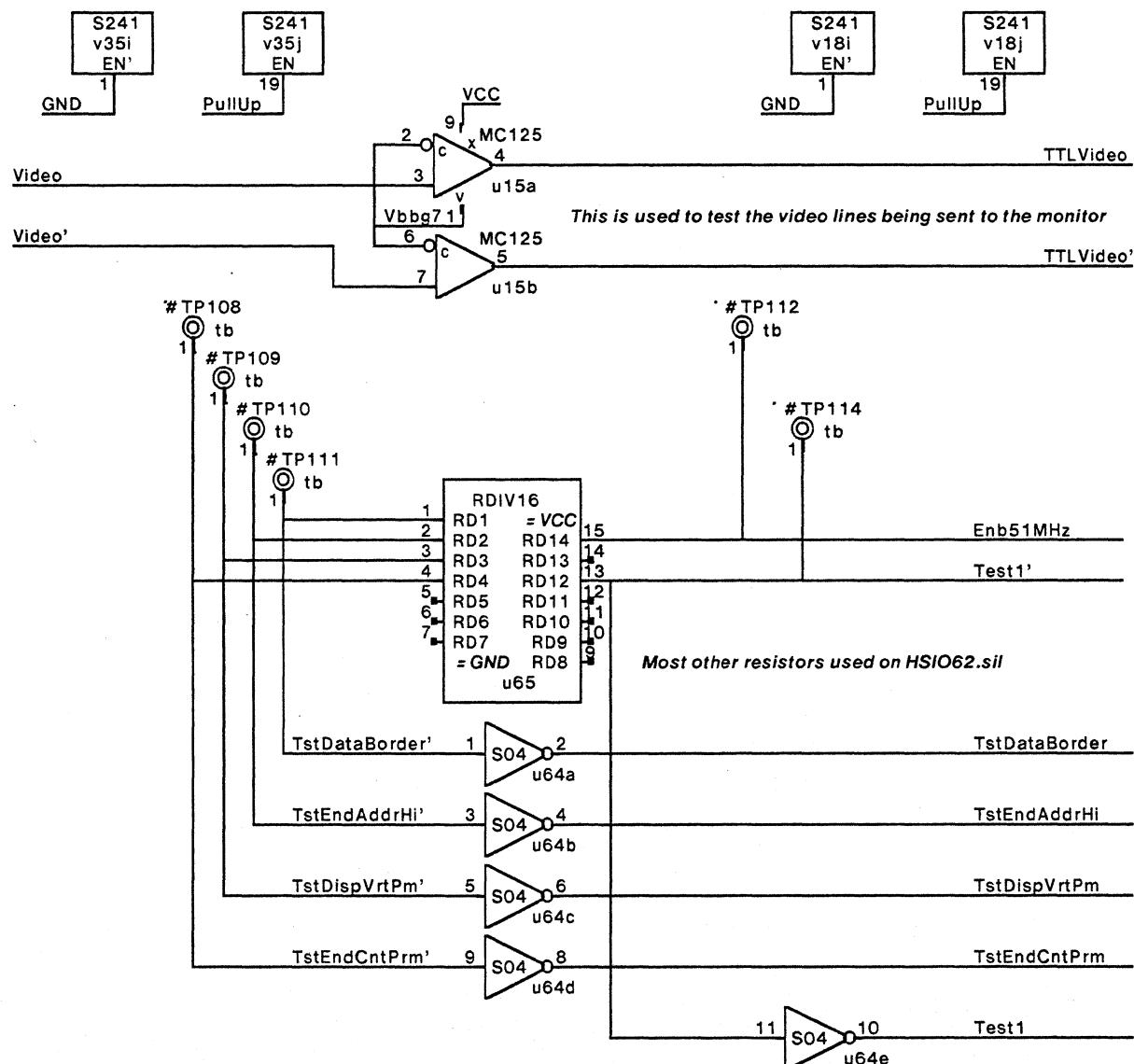
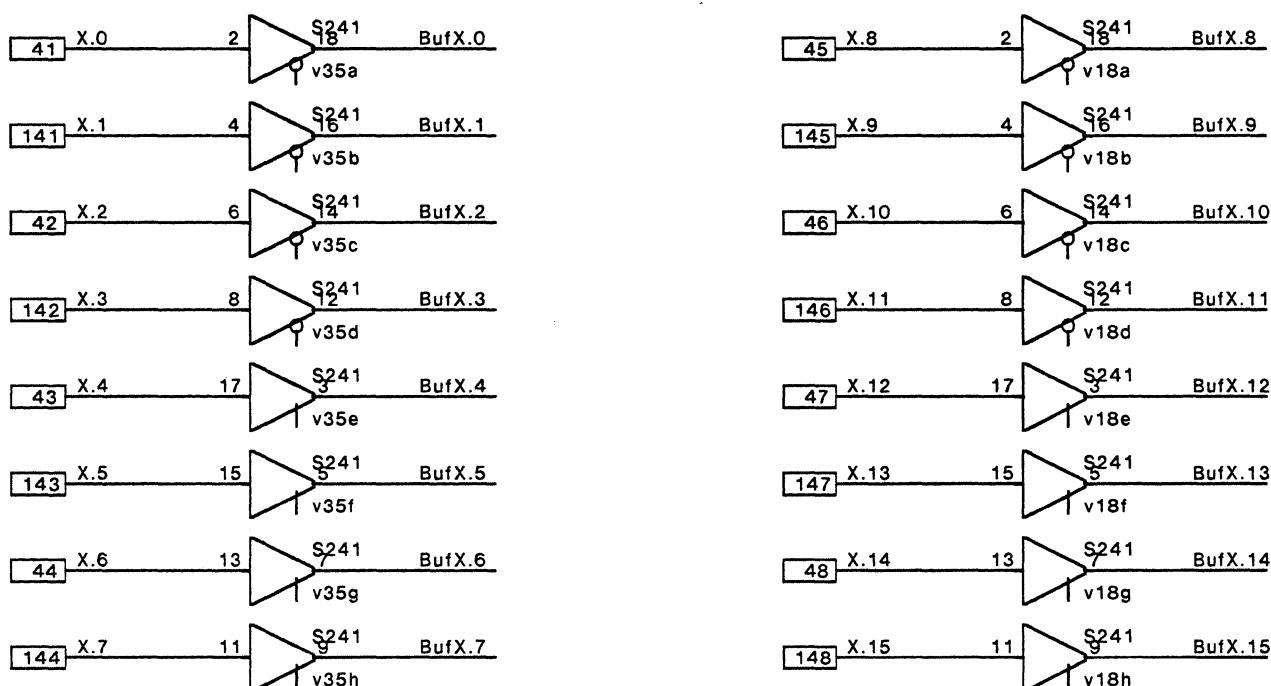


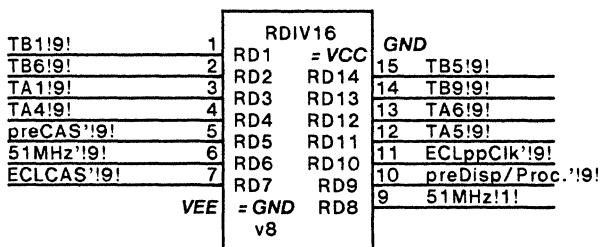
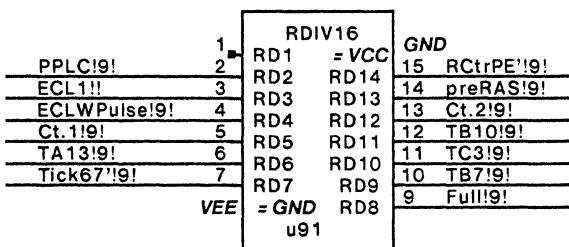
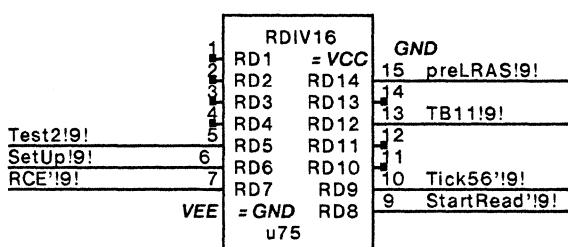
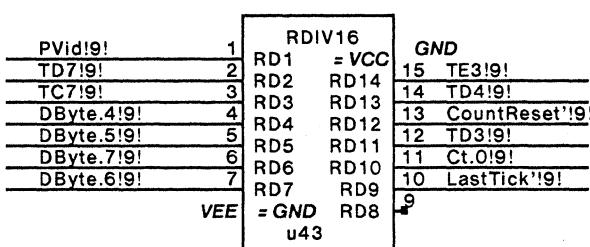
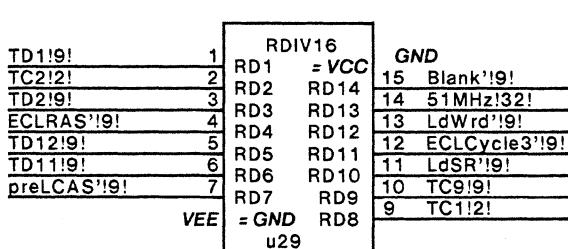
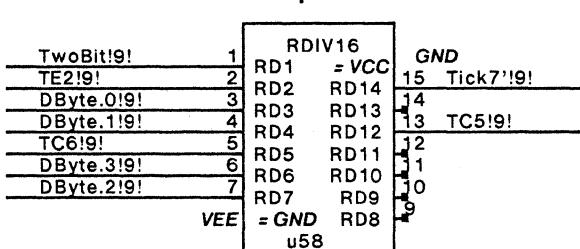
Terminators are shown on the clock page.

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS	DWG SIZE	DWG NO. 156P11448	SHEET REV.
	TITLE SCHEMATIC, HSIO	A4	SHEET 08 OF	B



Buffer X bus to reduce loading.



A**B****C****D****E****F**

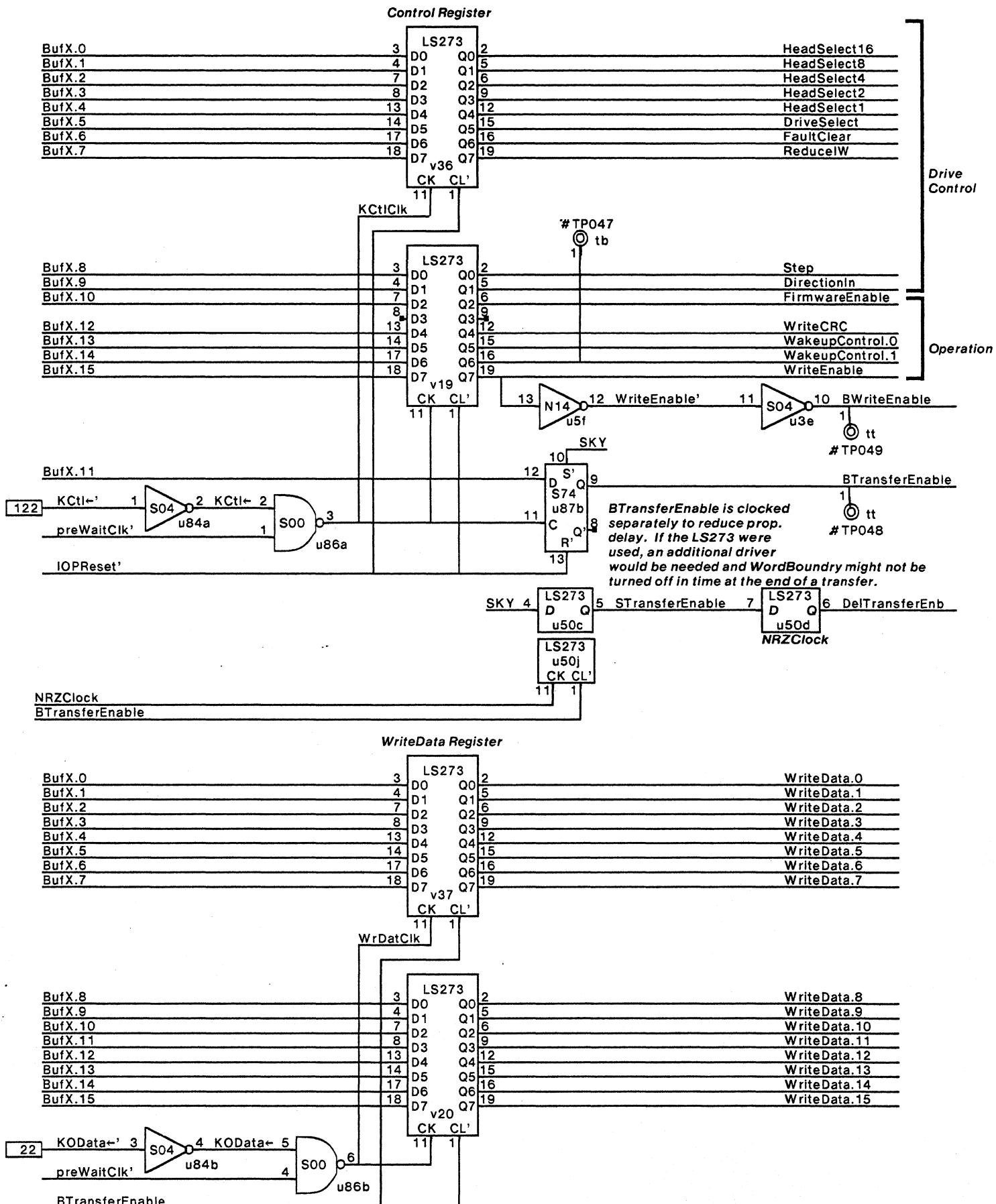
Termination Packages A, B, C, D, E above are
100 ohm termination to -2 V
Allen-Bradley part no. 316E161261

Pin 16 on each termination package is connected
to GND and Pin 8 to VEE (-5.2 V). This is done on
pWSD09.sil and sWSD09.sil where there is more room.
This connection make the termination compatible
with normal ECL power rules.

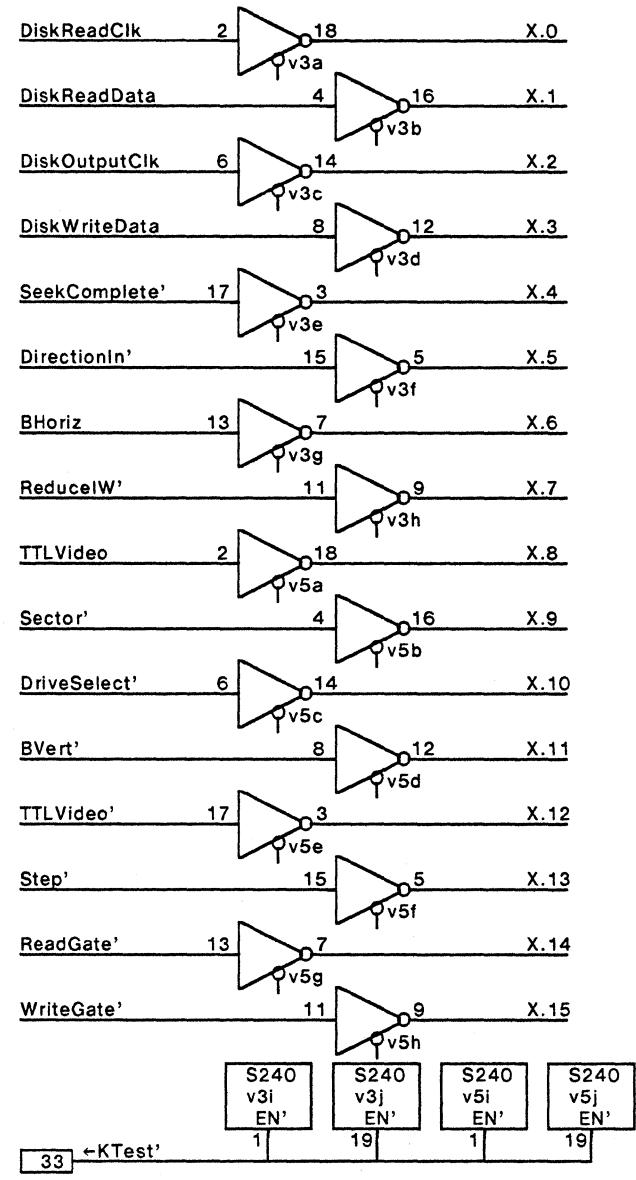
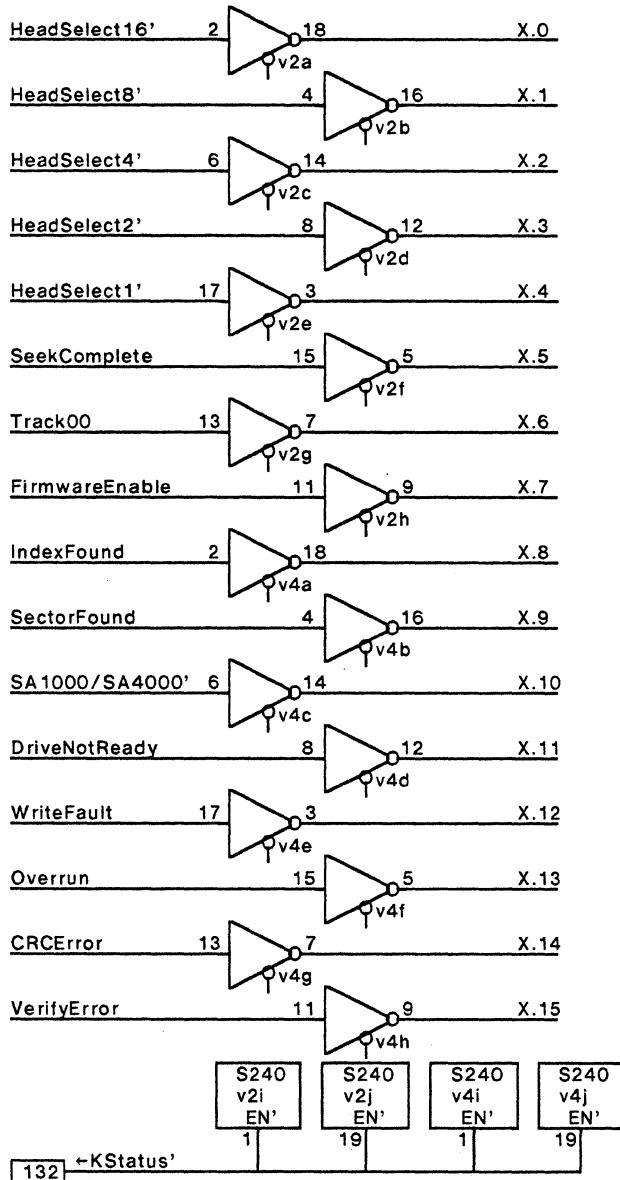
Note:

The prefix #% in front of chip position causes the chip to
be wired upside down in socket. This prevents cutting of
ground connections on stitchweld card.

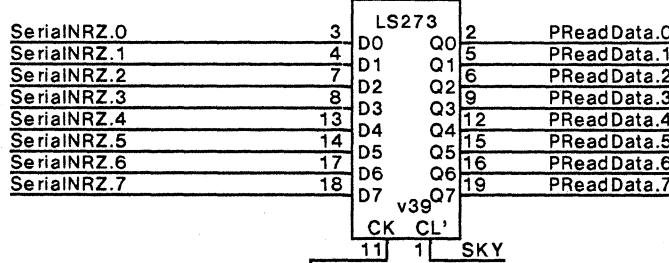
The suffix ! prevents Route from attempting automatic
terminator assignment since DO stitchweld card has none defined.
Subnet wiring order for a net is done by appending to the net name
a ! followed by the wiring sequence number of the node in the net.
Automatic terminator assignment is inhibited by use of ! as the
last character in the character string of the net. This must occur
after the subnet feature if it is also being used.



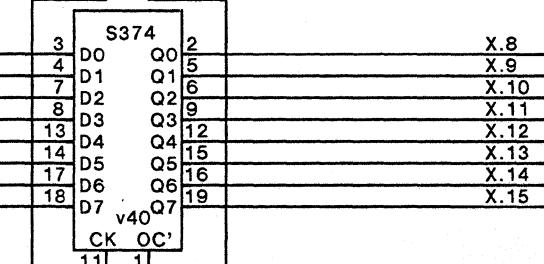
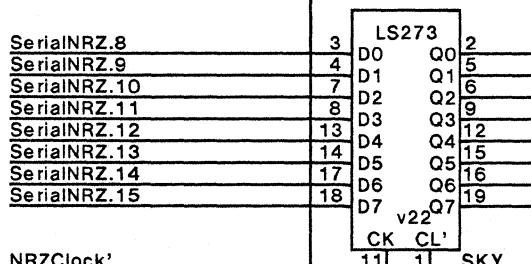
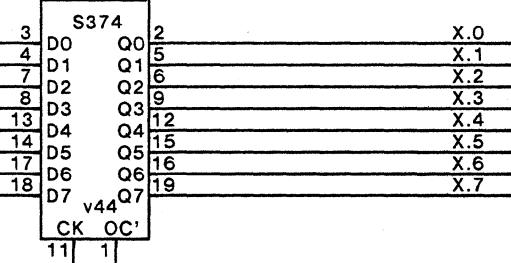
Status/Test Multiplexer



ReadData Buffer Register

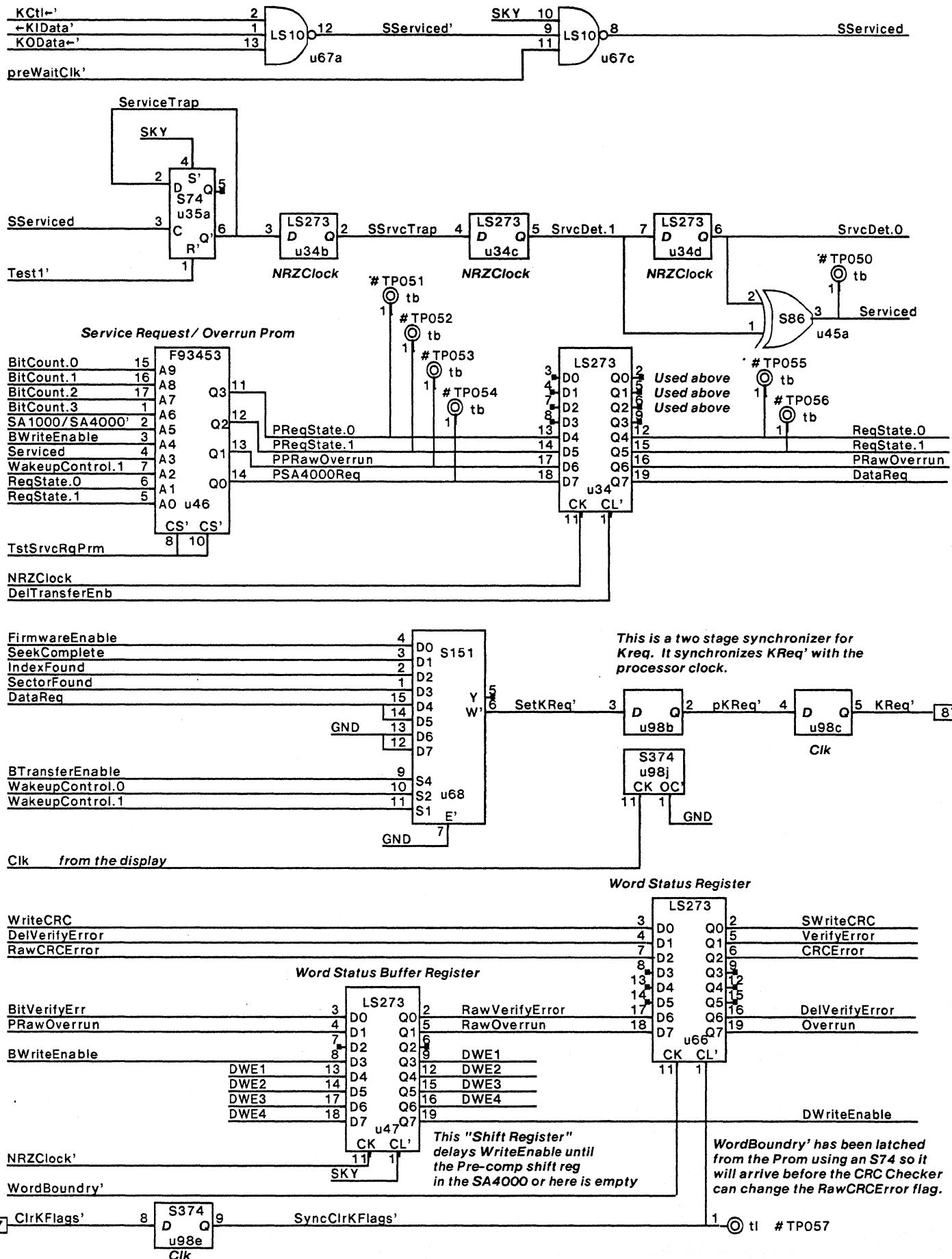


ReadData Register

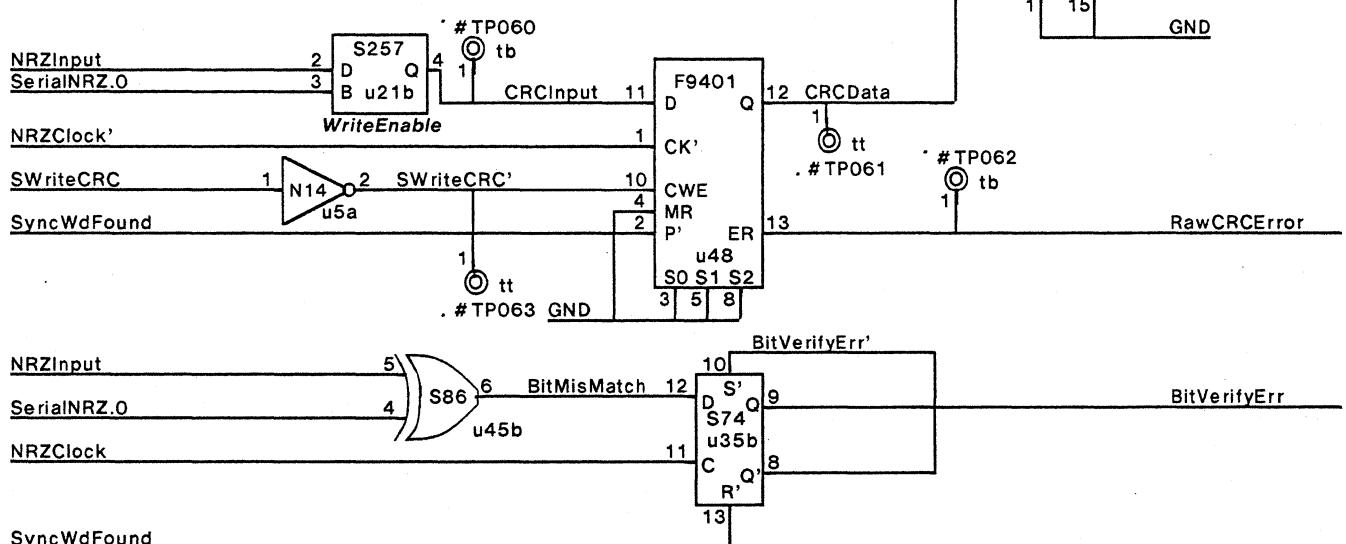
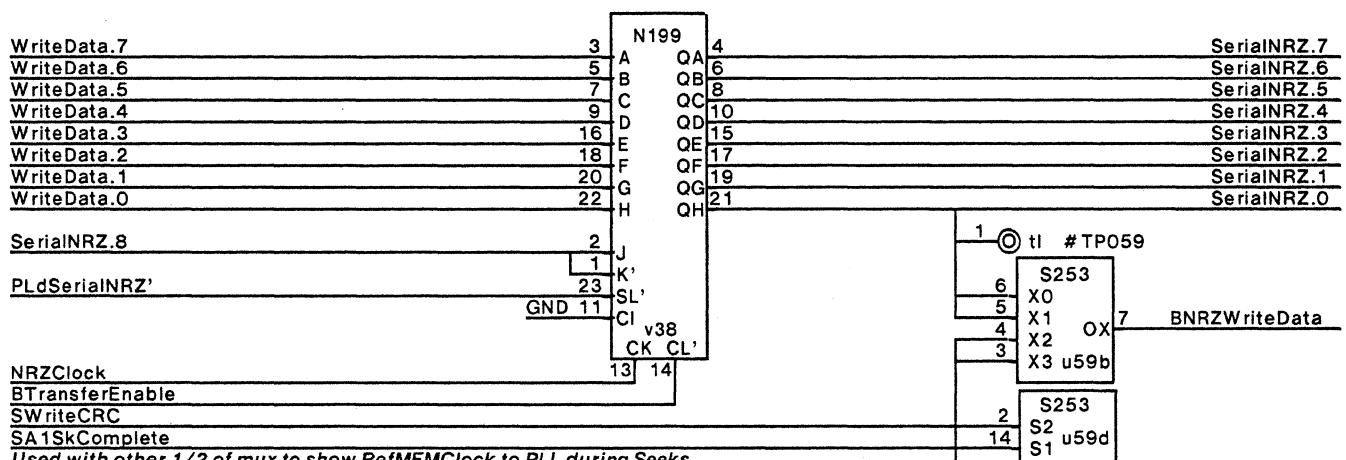
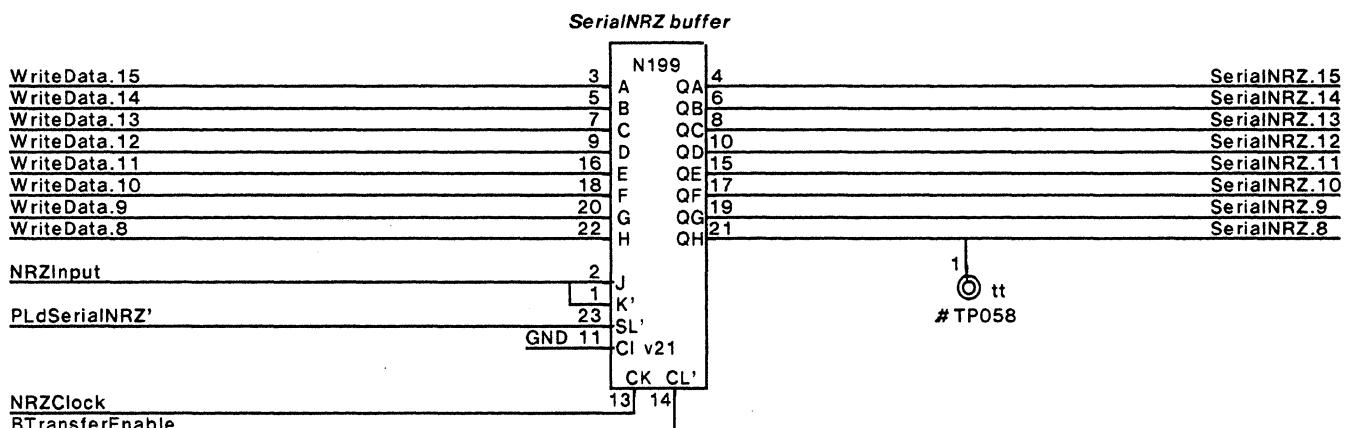


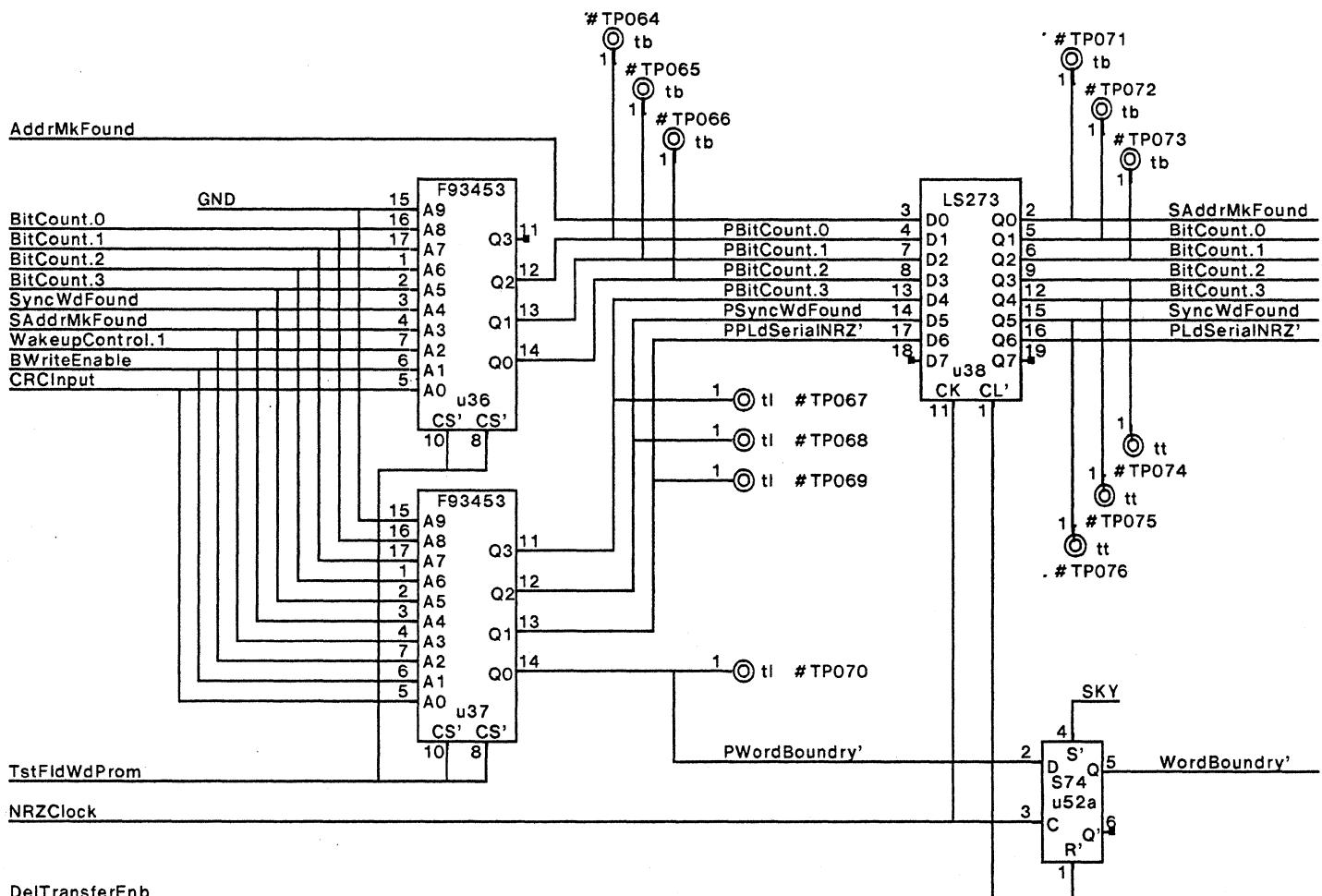
NRZClock'
WordBoundary'
→KIData'

32



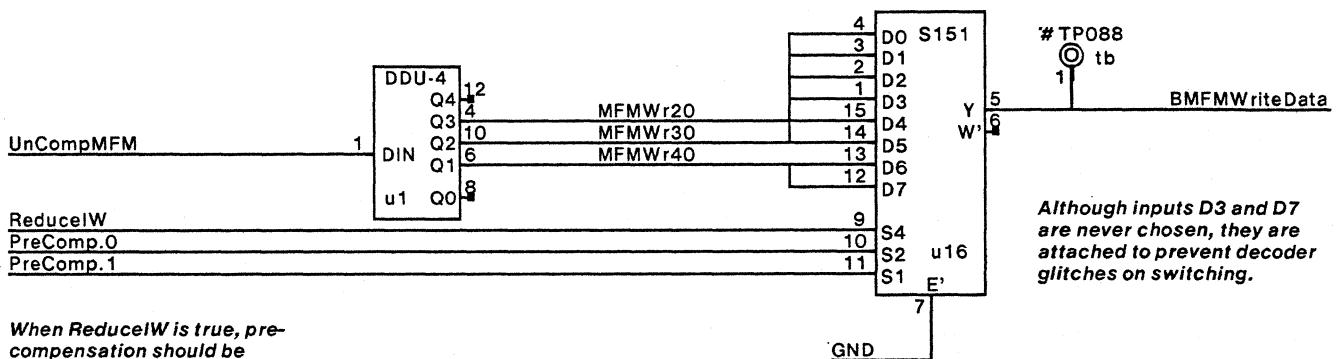
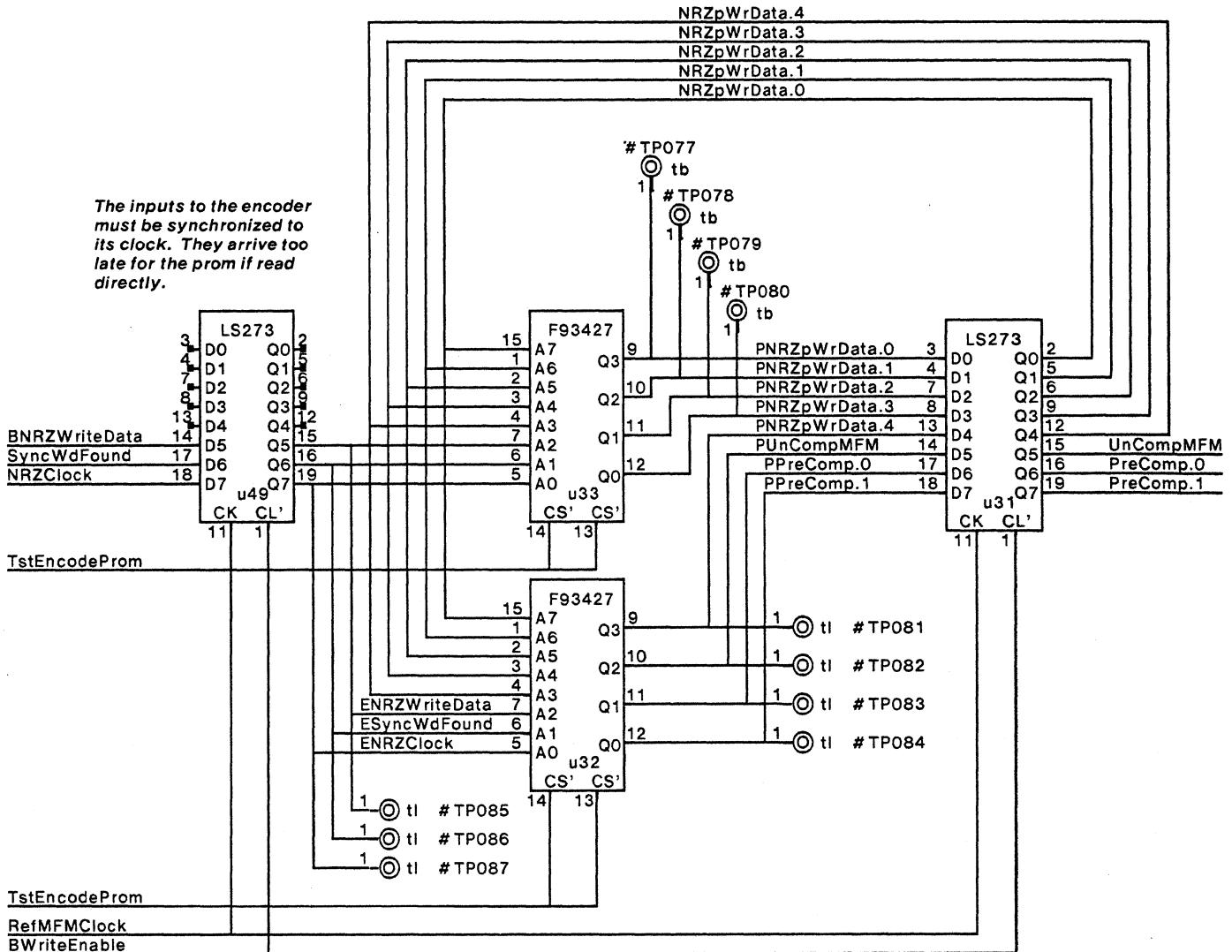
SerialNRZ Shift Register and Error Checking





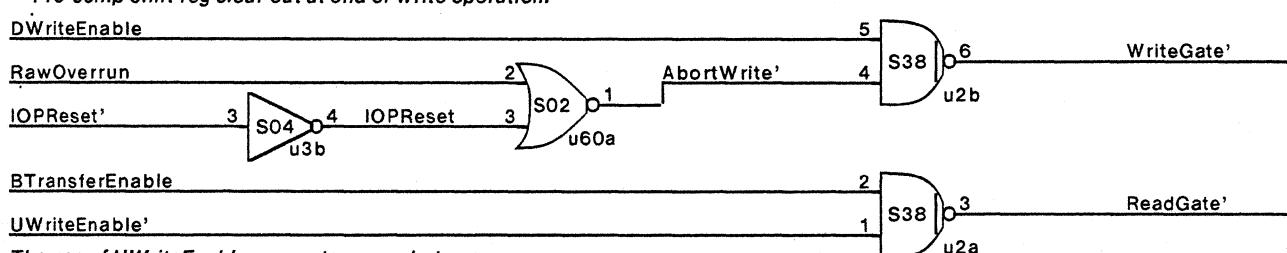
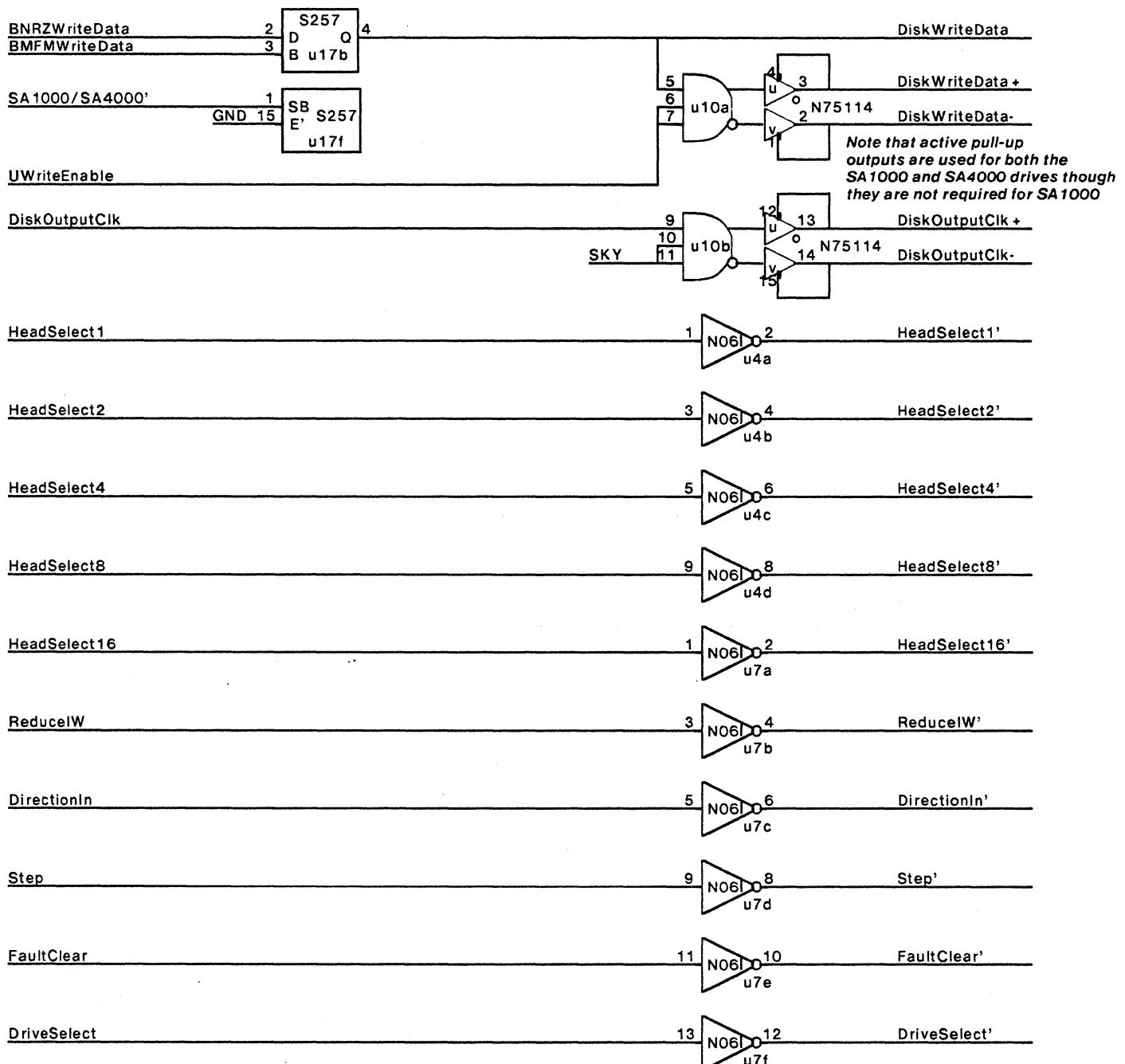
Using an S74 instead of the LS273 speeds up WordBoundary's so it will change before the RawCRCError indicator from the 9401 CRC Checker. This allows us to latch the CRCError signal directly using WordBoundary'. The RawCRCError signal is too slow to latch into the Word Status buffer register using NRZClock'. There is then a race between WordBoundary' and RawCRCError after NRZClock rises. Using the faster S74 here ensures WordBoundary' wins.

The inputs to the encoder must be synchronized to its clock. They arrive too late for the prom if read directly.

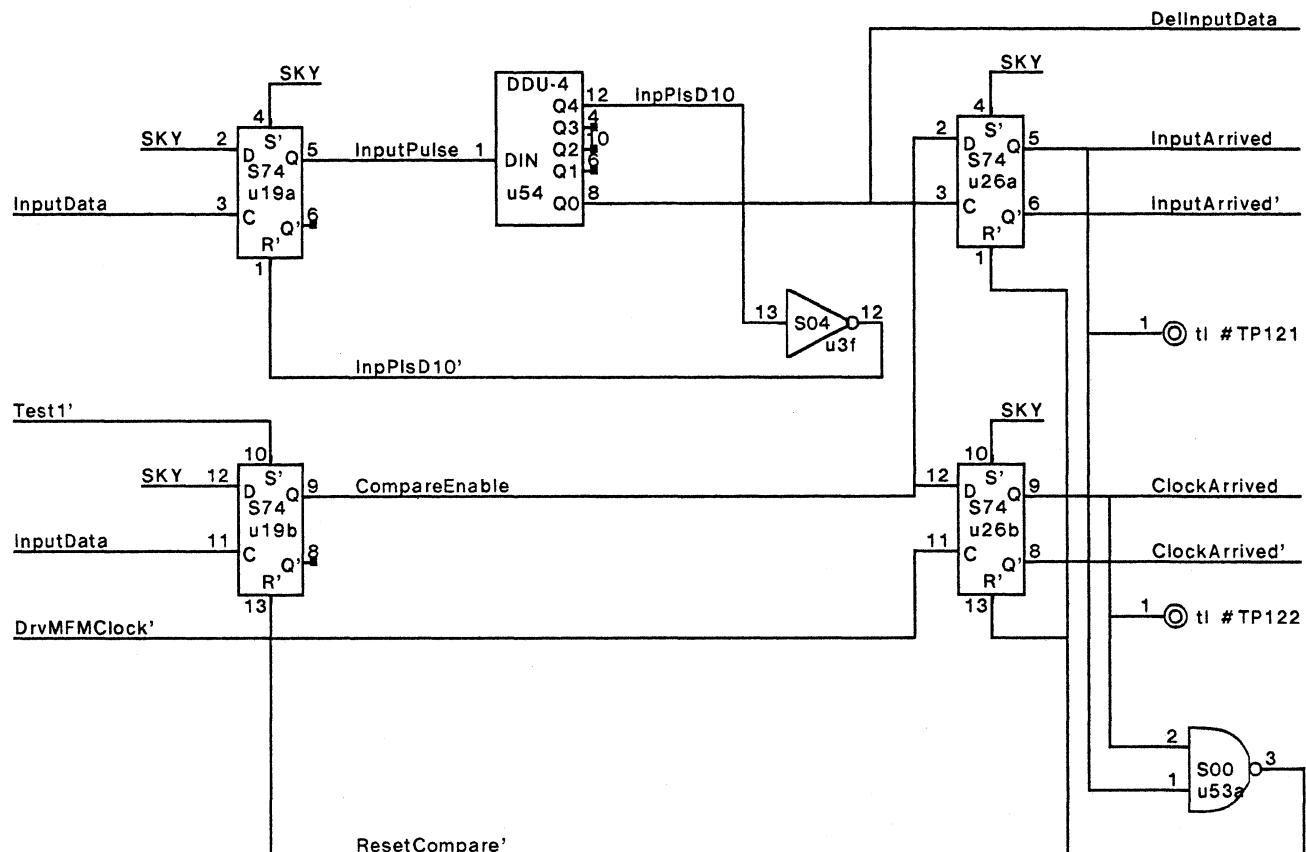


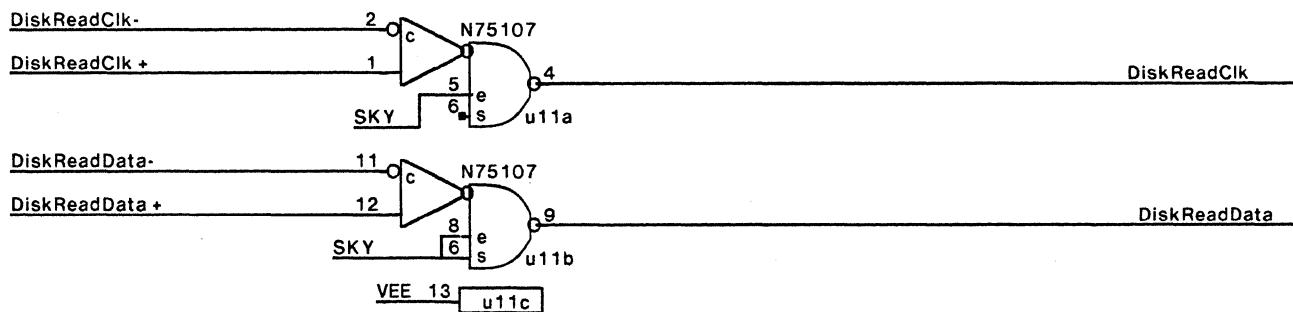
When *ReduceIW* is true, pre-compensation should be enabled (inner tracks).

Although inputs D3 and D7 are never chosen, they are attached to prevent decoder glitches on switching.

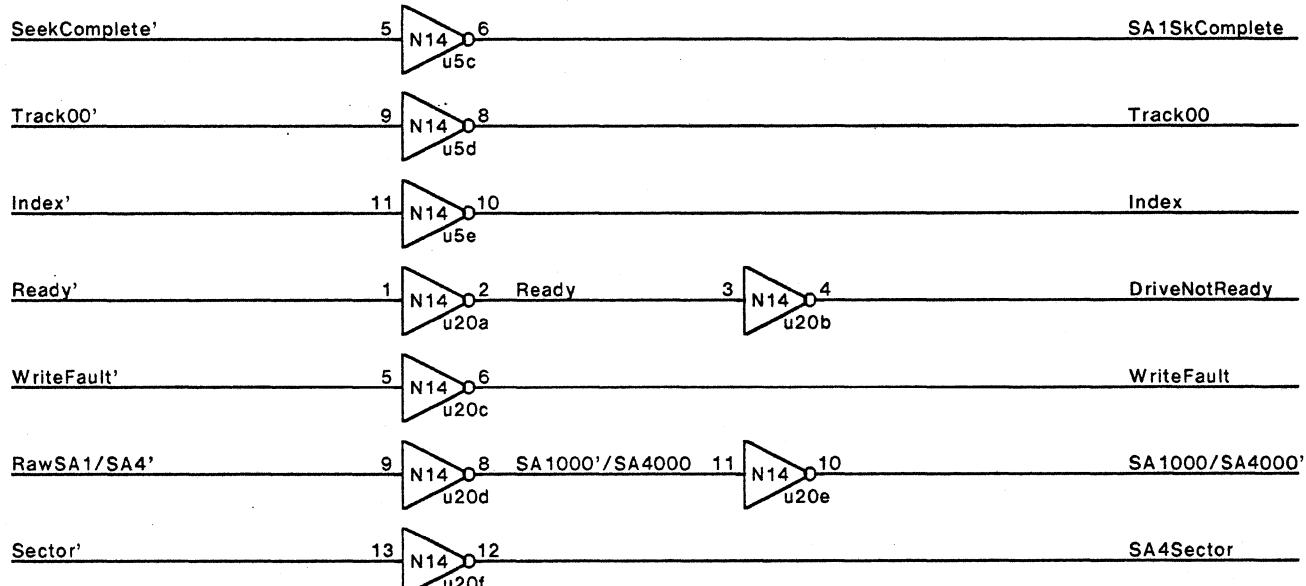
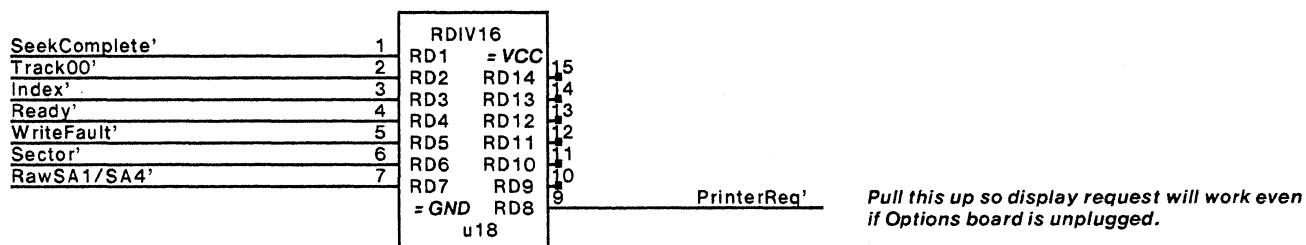


The use of UWriteEnable prevents a race between WriteGate' and ReadGate'. If BWriteEnable were used, there would be a race between BTransferEnable and BWriteEnable when finishing a write op that could glitch ReadGate', causing a WriteFault. Since BTransferEnable is faster than UWriteEnable, there is a ~20 ns glitch in ReadGate at the beginning of a Write Op. This causes NRZClock to pause, but only temporarily.

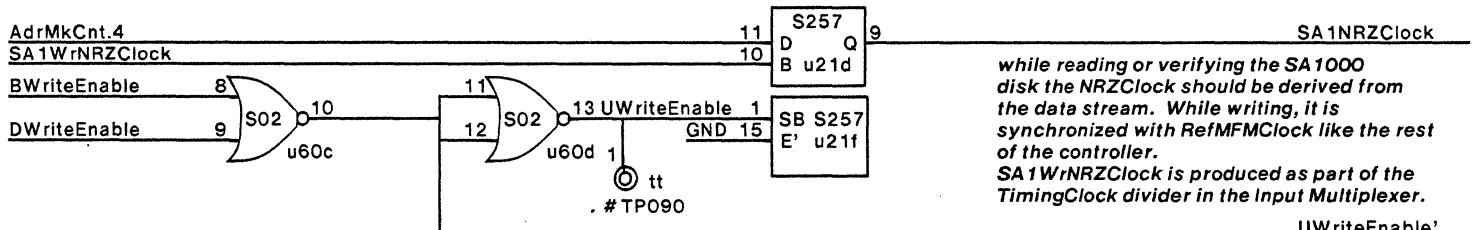
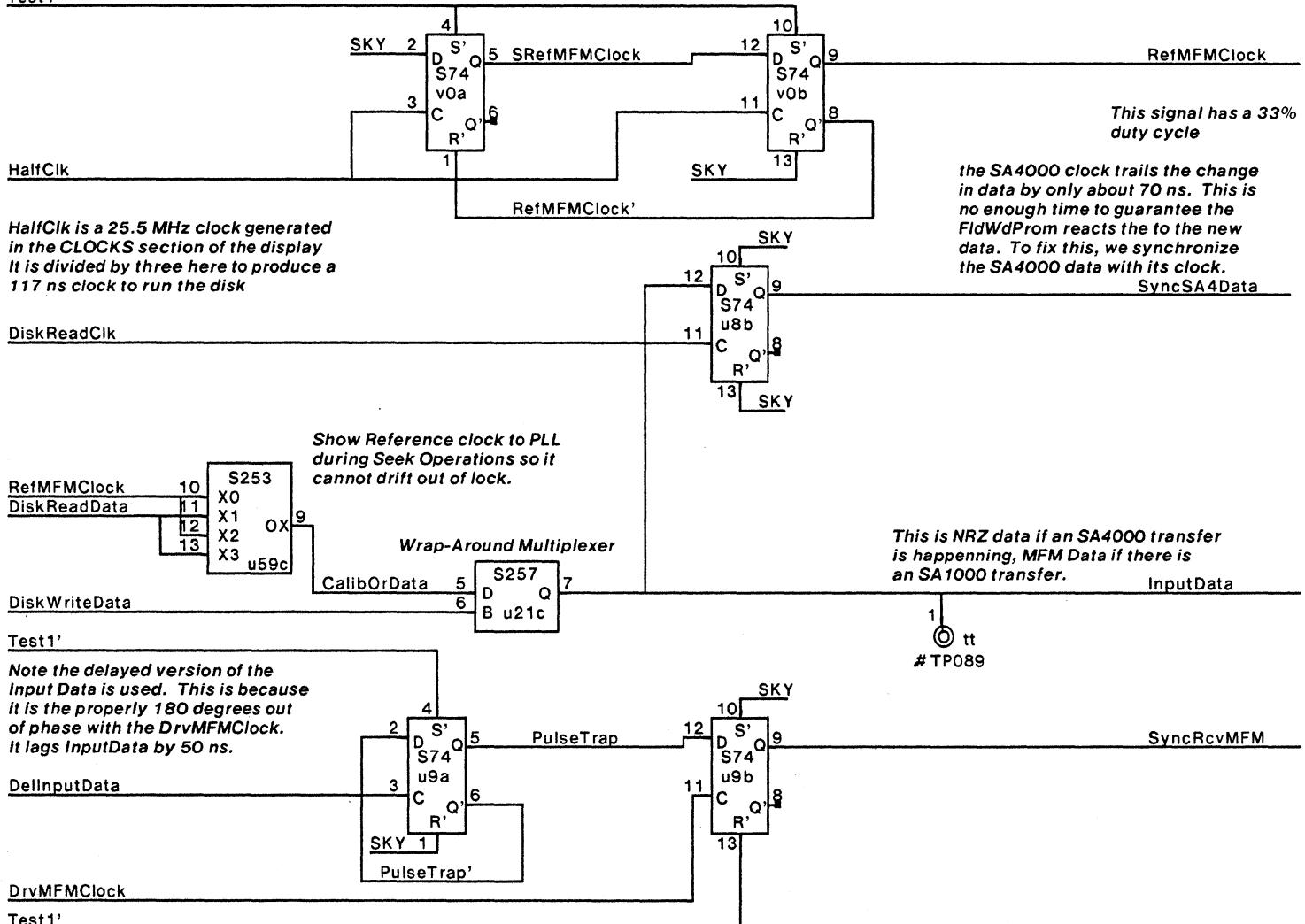




*This is a Beckman RPack number
898-5-R220/330.*

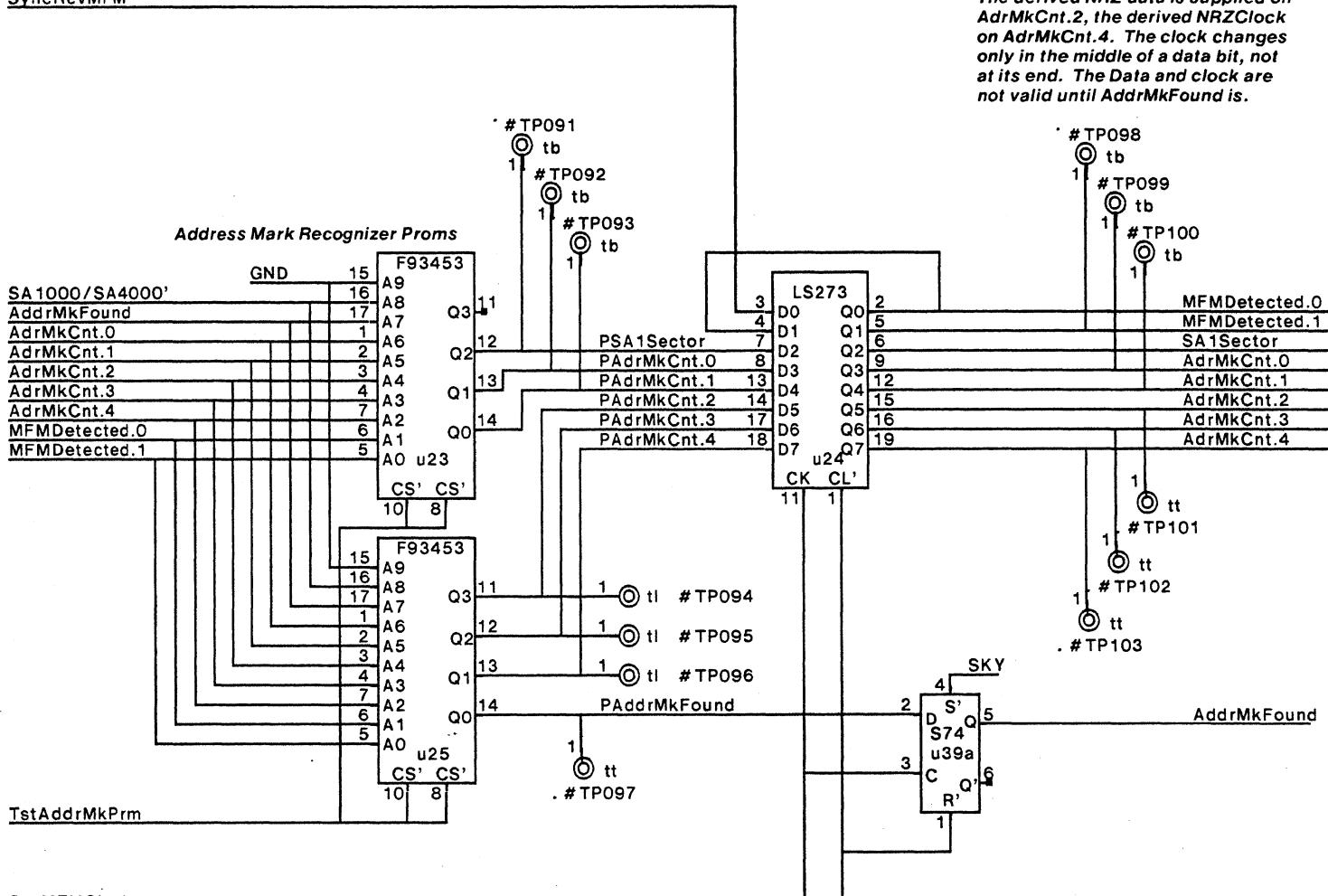


Test1'

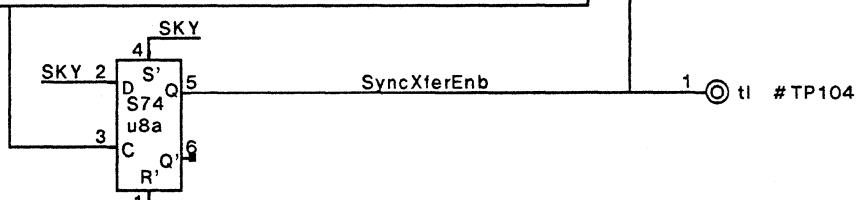


We note that AdrMkCnt.4 ceases to be active when TransferEnable drops. A clock is needed to start a write operation, so SA1NRZClock is set to the always active SA1WrNRZClock as soon as WriteEnable goes active. To ensure the DWriteEnable shift register delay is cleared, we keep SA1NRZClock set to SA1WrNRZClock until DWriteEnable goes lo.

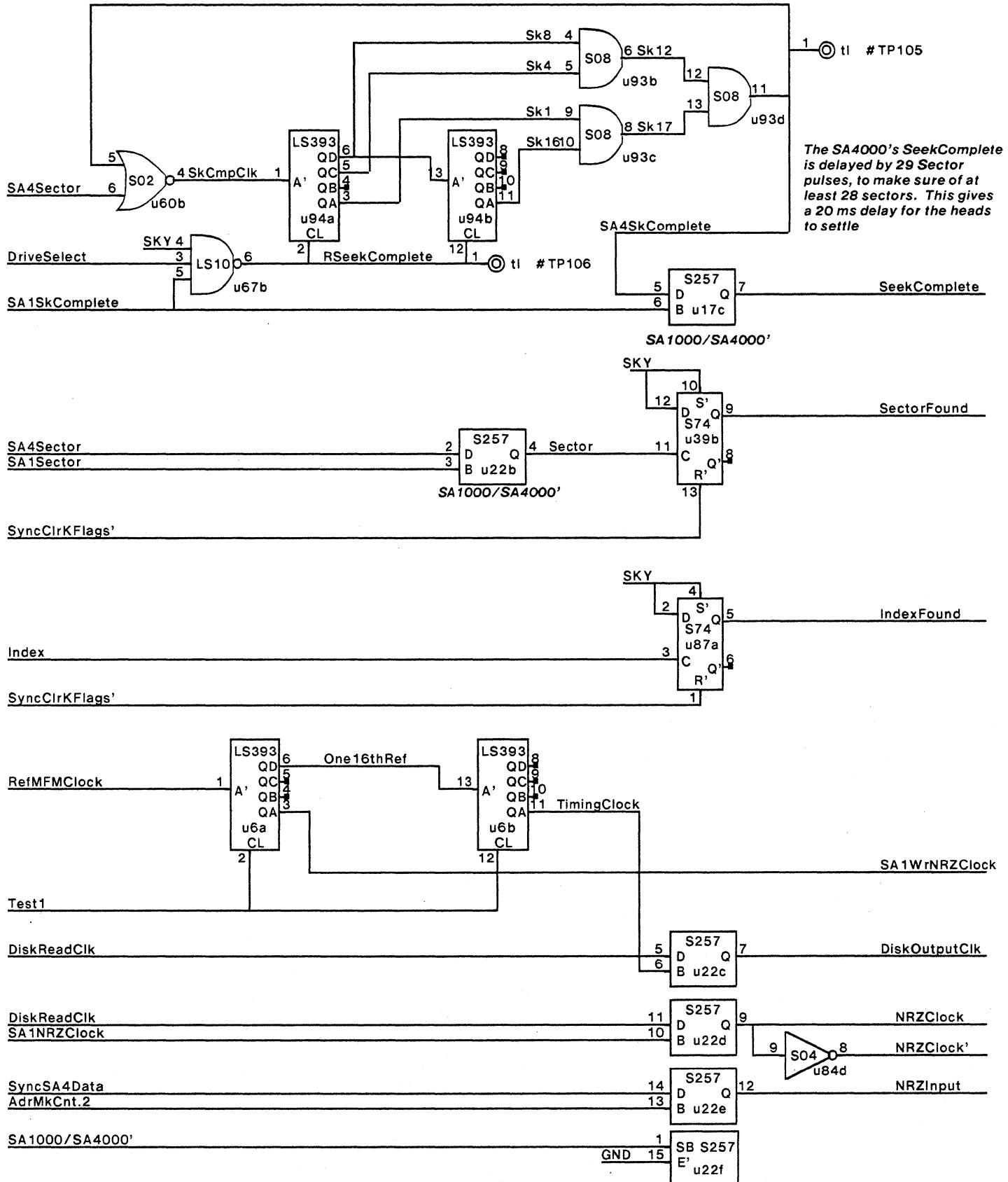
SyncRcvMFM



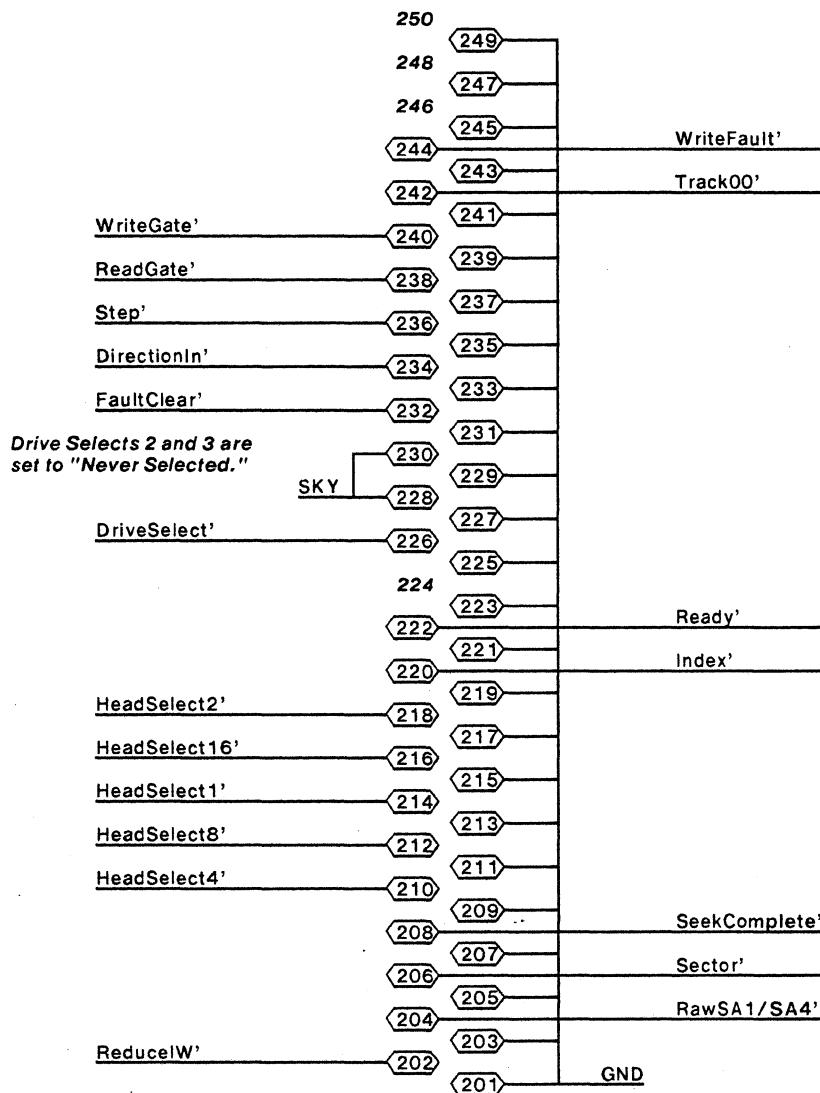
DrvMFMClock



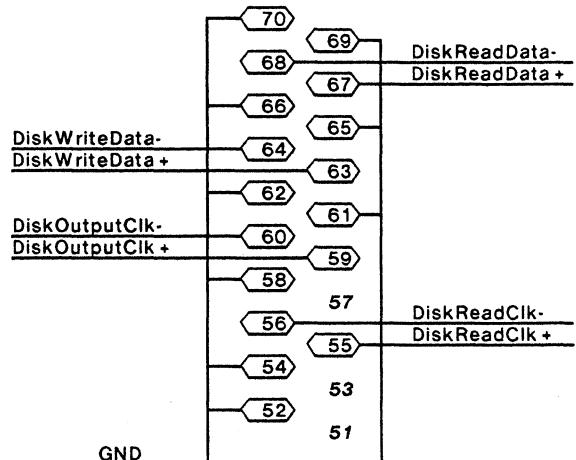
BTtransferEnable



This 50 pin connector is in location D of the HSIO board.



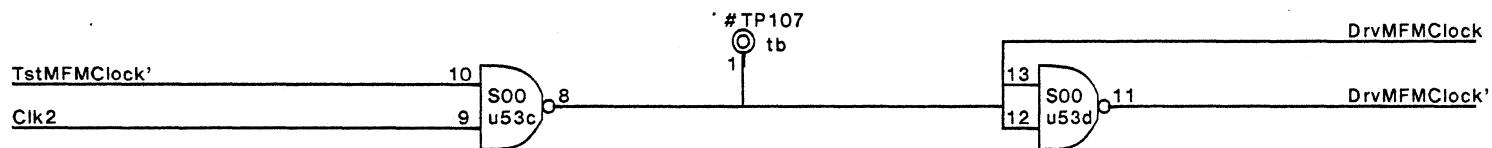
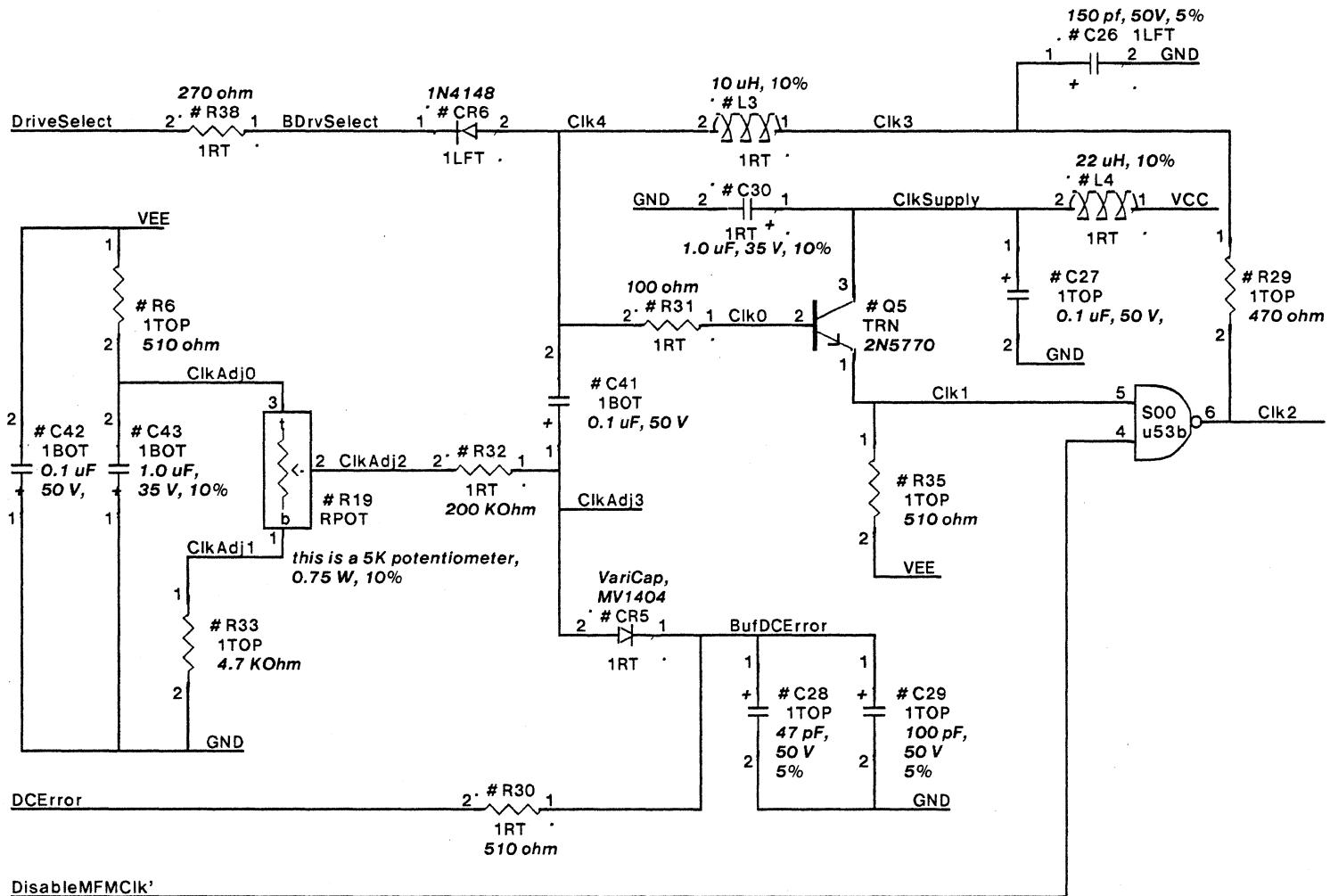
this 20 pin connector occupies position C on the HSIO board.



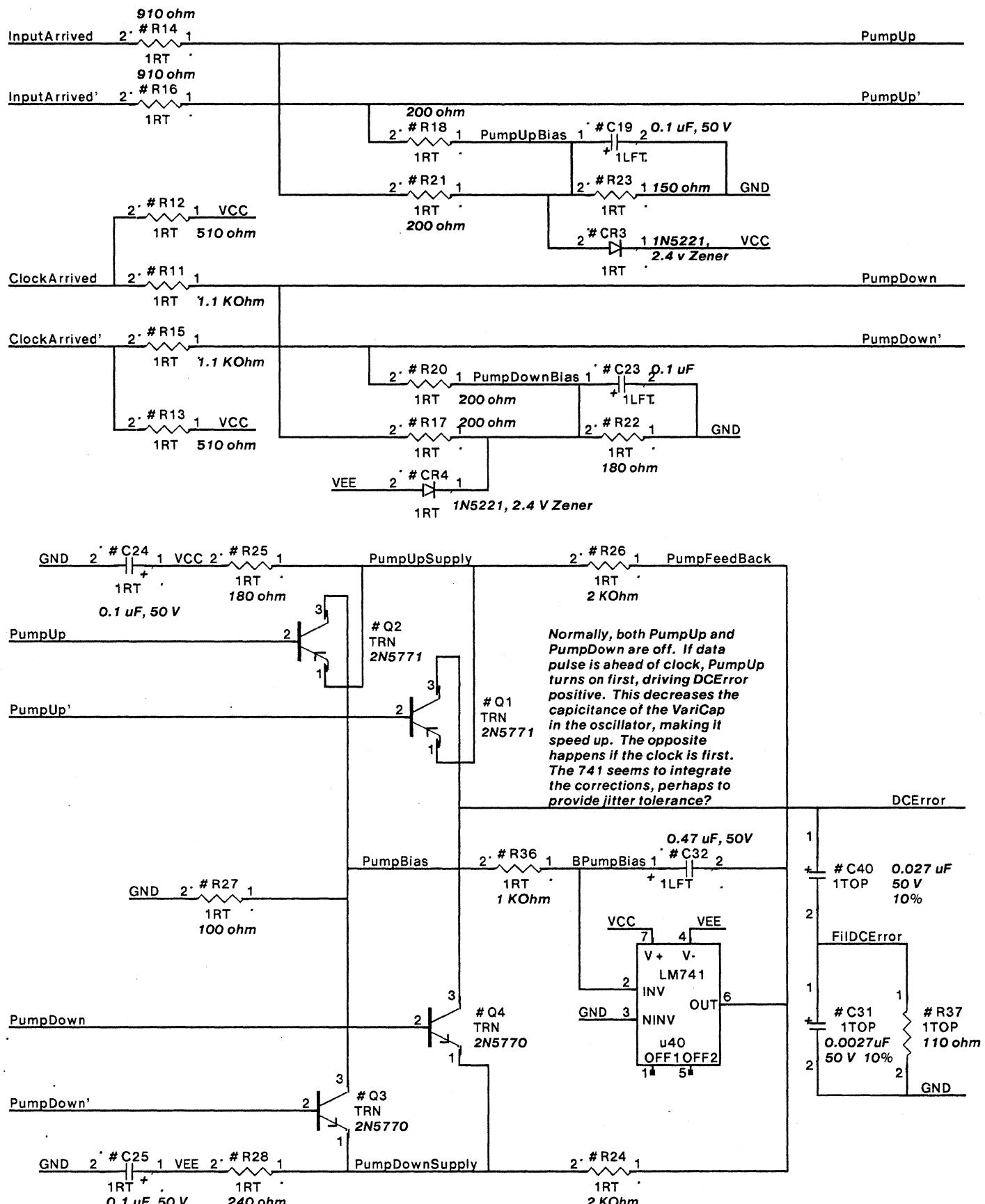
DiskReadClk +	1' 1 FT 2 # R2	51 ohm, 10%
DiskReadClk -	1' 1 FT 2 # R3	51 ohm, 10%
DiskReadData +	1' 1 FT 2 # R4	51 ohm 10%
DiskReadData -	1' 1 FT 2 # R5	GND 51 ohm, 10%

This resistor supplies logical one to the board
It is also 51 ohms

VCC 1' 1 FT 2 # R1 SKY

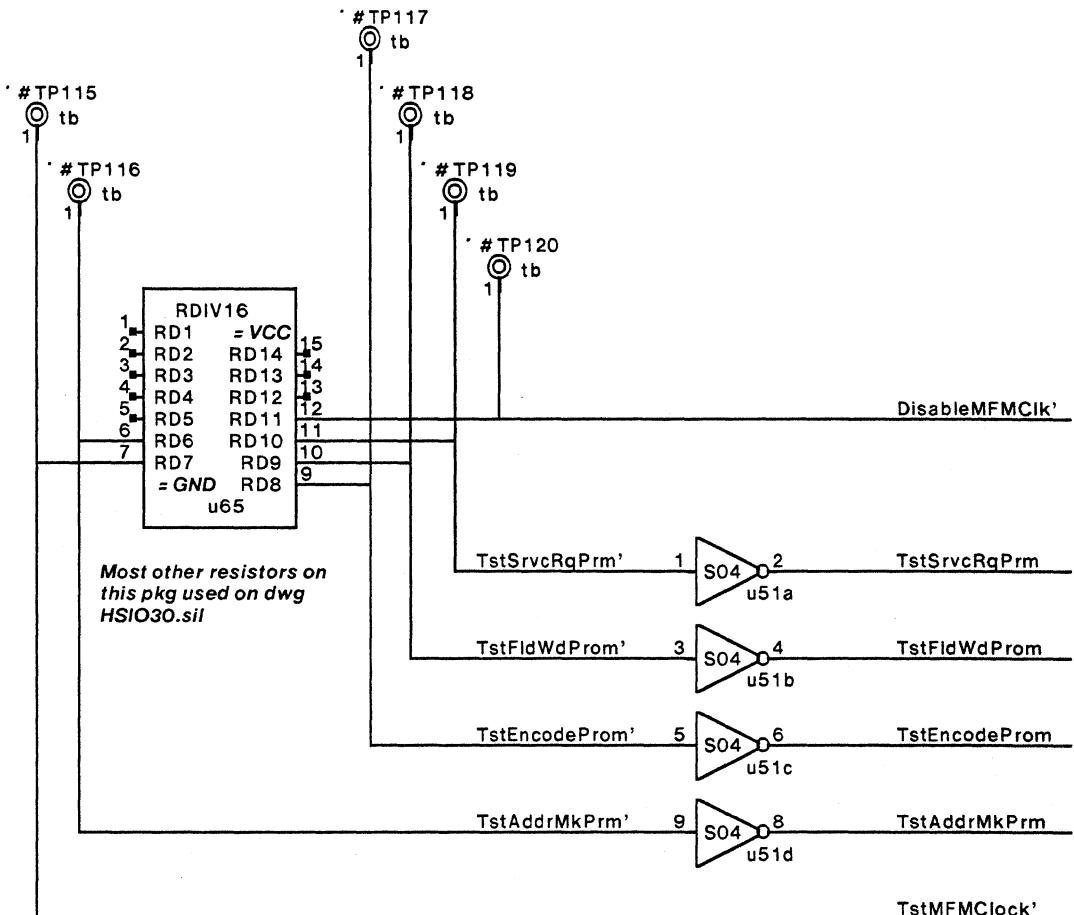


All resistors shown above are 0.25 watt, 5% parts



All resistors shown are 0.25 watt, 5% parts. All capacitors shown on this page have 10% tolerances.

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS		DWG NO. 156P11448	SHEET REV.
	TITLE	SCHEMATIC, HSIO		
	DWG SIZE		SHEET 26 OF	B



VEE

1	#C1 ₂	1LFT .
1	#C10 ₂	1LFT .
1	#C11 ₂	1LFT .
1	#C20 ₂	1LFT .
1	#C21 ₂	1LFT .
1	#C22 ₂	1LFT .
1	#C33 ₂	1LFT .
1	#C34 ₂	1LFT .
1	#C35	1LFT .
1	#C44 ₂	1LFT .
1	#C45 ₂	1LFT .
1	#C53 ₂	1LFT .
1	#C54 ₂	1LFT .
1	#C55 ₂	1LFT .
1	#C61 ₂	1LFT .
1	#C62 ₂	1LFT .
1	#C71 ₂	1LFT .
1	#C72 ₂	1LFT .
1	#C78 ₂	1LFT .

VCC

1	#C4 ₂	1LFT .
1	#C5 ₂	1LFT .
1	#C6 ₂	1LFT .
1	#C7 ₂	1LFT .
1	#C8 ₂	1LFT .
1	#C9 ₂	1LFT .
1	#C12 ₂	1LFT .
1	#C13 ₂	1LFT .
1	#C14 ₂	1LFT .
1	#C15 ₂	1LFT .
1	#C16 ₂	1LFT .
1	#C17 ₂	1LFT .
1	#C18 ₂	1LFT .
1	#C36 ₂	1LFT .
1	#C37 ₂	1LFT .
1	#C38 ₂	1LFT .
1	#C39 ₂	1LFT .

1	#C46 ₂	1LFT .
1	#C47 ₂	1LFT .
1	#C48 ₂	1LFT .
1	#C49 ₂	1LFT .
1	#C50 ₂	1LFT .
1	#C51 ₂	1LFT .
1	#C52 ₂	1LFT .
1	#C56 ₂	1LFT .
1	#C57 ₂	1LFT .
1	#C58 ₂	1LFT .
1	#C59 ₂	1LFT .
1	#C60 ₂	1LFT .
1	#C63 ₂	1LFT .
1	#C64 ₂	1LFT .
1	#C65 ₂	1LFT .
1	#C66 ₂	1LFT .
1	#C67 ₂	1LFT .
1	#C68 ₂	1LFT .
1	#C69 ₂	1LFT .

1	#C70 ₂	1LFT .
1	#C73 ₂	1LFT .
1	#C74 ₂	1LFT .
1	#C75 ₂	1LFT .
1	#C76 ₂	1LFT .
1	#C77 ₂	1LFT .
1	#C79 ₂	1LFT .
1	#C80 ₂	1LFT .
1	#C81 ₂	1LFT .
1	#C82 ₂	1LFT .
1	#C83 ₂	1LFT .
1	#C84 ₂	1LFT .
1	#C85 ₂	1LFT .
1	#C86 ₂	1LFT .
1	#C87 ₂	1LFT .
1	#C88 ₂	1LFT .
1	#C89 ₂	1LFT .
1	#C90 ₂	1LFT .
1	#C91 ₂	1LFT .

GND

NOTE: PART ID--702W05218, CAP., CERAM, +80-20% 50V .10UF

XEROX	PROPRIETARY NOTE ON COVER SHEET APPLIES TO ALL SHEETS		DWG SIZE A4	DWG NO. 156P11448		SHEET REV. B
	TITLE	SCHEMATIC, HSIO		SHEET	28	

Comments:

- 1) Designator notation notes: u1-99 = U1-99, v0-99 = U100-199, w0-99 = U200-299
- 2) The last item on lines below, preceded by a semicolon (;), is the schematic page number on which the test point, connector or signal information originates.
- 3) Line with no page number was a continuation of the previous line.

#TP001	.1i	VCC	:01	#TP060	.1i	CRCInput	;15
#TP002	.1i	VEE	:01	#TP061	.1i	CRCData	;15
#TP003	.1i	Test2	:02	#TP062	.1i	RawCRCError	;15
#TP004	.1i	BpCycle.3	:03	#TP063	.1i	SWriteCRC'	;15
#TP005	.1i	PPicSync	:04	#TP064	.1i	PBitCount.0	;16
#TP006	.1i	HighDataOut	:04	#TP065	.1i	PBitCount.1	;16
#TP007	.1i	LowDataOut	:04	#TP066	.1i	PBitCount.2	;16
#TP008	.1i	HighBorderOut	:04	#TP067	.1i	PBitCount.3	;16
#TP009	.1i	LowBorderOut	:04	#TP068	.1i	PSyncWdFound	;16
#TP010	.1i	pPHoriz'	:04	#TP069	.1i	PPLdSerialNRZ'	;16
#TP011	.1i	pPB1k	:04	#TP070	.1i	PWordBoundry'	;16
#TP012	.1i	pPD/P	:04	#TP071	.1i	SAddrMkFound	;16
#TP013	.1i	pPPic	:04	#TP072	.1i	BitCount.0	;16
#TP014	.1i	pVtClk	:04	#TP073	.1i	BitCount.1	;16
#TP015	.1i	pCDFifo	:04	#TP074	.1i	BitCount.2	;16
#TP016	.1i	pPReq'	:04	#TP075	.1i	BitCount.3	;16
#TP017	.1i	pNil	:04	#TP076	.1i	SyncWdFound	;16
#TP018	.1i	Pic	:04	#TP077	.1i	PNRZpWrData.0	;17
#TP019	.1i	B1k	:04	#TP078	.1i	PNRZpWrData.1	;17
#TP028	.1i	EndAddr.10	:06	#TP079	.1i	PNRZpWrData.2	;17
#TP029	.1i	EndAddr.11	:06	#TP080	.1i	PNRZpWrData.3	;17
#TP030	.1i	EndAddr.12	:06	#TP081	.1i	PNRZpWrData.4	;17
#TP031	.1i	EndAddr.13	:06	#TP082	.1i	PUnCompMFM	;17
#TP032	.1i	EndAddr.14	:06	#TP083	.1i	PPreComp.0	;17
#TP033	.1i	EndAddr.15	:06	#TP084	.1i	PPreComp.1	;17
#TP034	.1i	EndSeg	:07	#TP085	.1i	ENRZWriteData	;17
#TP035	.1i	A63Ct	:07	#TP086	.1i	ESyncWdFound	;17
#TP036	.1i	LoDAddrCarry	:07	#TP087	.1i	ENRZClock	;17
#TP037	.1i	WC.0	:07	#TP088	.1i	BMFMWriteData	;17
#TP038	.1i	WC.1	:07	#TP089	.1i	InputData	;21
#TP039	.1i	WC.2	:07	#TP090	.1i	UWriteEnable	;21
#TP040	.1i	EndRndRead'	:07	#TP091	.1i	PSA1Sector	;22
#TP041	.1i	PCt.0	:07	#TP092	.1i	PAdrMkCnt.0	;22
#TP042	.1i	PCt.1	:07	#TP093	.1i	PAdrMkCnt.1	;22
#TP043	.1i	PCt.2	:07	#TP094	.1i	PAdrMkCnt.2	;22
#TP044	.1i	ECt.0	:07	#TP095	.1i	PAdrMkCnt.3	;22
#TP045	.1i	ECt.1	:07	#TP096	.1i	PAdrMkCnt.4	;22
#TP046	.1i	ECt.2	:07	#TP097	.1i	PAddrMkFound	;22
#TP047	.1i	WakeupControl.1	:12	#TP098	.1i	MFDetected.1	;22
#TP048	.1i	BTransferEnable	:12	#TP099	.1i	AdrMkCnt.0	;22
#TP049	.1i	BWriteEnable	:12	#TP100	.1i	AdrMkCnt.1	;22
#TP050	.1i	Serviced	:14	#TP101	.1i	AdrMkCnt.2	;22
#TP051	.1i	PReqState.0	:14	#TP102	.1i	AdrMkCnt.3	;22
#TP052	.1i	PReqState.1	:14	#TP103	.1i	AdrMkCnt.4	;22
#TP053	.1i	PPRawOverrun	:14	#TP104	.1i	SyncXferEnb	;22
#TP054	.1i	PSA4000Req	:14	#TP106	.1i	RSeekComplete	;23
#TP055	.1i	ReqState.0	:14	#TP107	.1i	DrvMFMClock	;25
#TP056	.1i	ReqState.1	:14	#TP108	.1i	TstEndCntPrm'	;10
#TP058	.1i	SerialNRZ.8	:15	#TP109	.1i	TstDispVrtPm'	;10
#TP059	.1i	SerialNRZ.0	:15	#TP110	.1i	TstEndAddrHi'	;10
				#TP111	.1i	TstDataBorder'	;10
				#TP112	.1i	Enb51MHz	;10

#TP113	.1i Gated51MHz'	;09	C223	GND	;24
#TP114	.1i Test1'	;10	C225	GND	;24
#TP115	.1i TstMFMClock'	;27	C226	DriveSelect'	;24
#TP116	.1i TstAddrMkPrm'	;27	C227	GND	;24
#TP117	.1i TstEncodeProm'	;27	C228	SKY	;24
#TP118	.1i TstFldWdProm'	;27	C229	GND	;24
#TP119	.1i TstSrvcRqPrm'	;27	C230	SKY	;24
#TP120	.1i DisableMFMClk'	;27	C231	GND	;24
#TP121	.1i InputArrived	;19	C232	FaultClear'	;24
#TP122	.1i ClockArrived	;19	C233	GND	;24
			C234	DirectionIn'	;24
C001	HSync	;09	C235	GND	;24
C002	GND	;09	C236	Step'	;24
C003	VSync'	;09	C237	GND	;24
C004	GND	;09	C238	ReadGate'	;24
C005	Video	;09	C239	GND	;24
C006	Video'	;09	C240	WriteGate'	;24
C007	GND	;09	C241	GND	;24
C008	VEE	;09	C242	Track00'	;24
C009	GND	;09	C243	GND	;24
C052	GND	;24	C244	WriteFault'	;24
C054	GND	;24	C245	GND	;24
C055	DiskReadClk+	;24	C247	GND	;24
C056	DiskReadClk-	;24	C249	GND	;24
C058	GND	;24			
C059	DiskOutputClk+	;24	E002	Cycle.1'	;03
C060	DiskOutputClk-	;24	E003	Cycle.2'	;03
C061	GND	;24	E004	Cycle.3'	;03
C062	GND	;24	E005	RAS'	;02
C063	DiskWriteData+	;24	E006	CAS	;02
C064	DiskWriteData-	;24	E007	WPulse	;02
C065	GND	;24	E009	ppClk	;02
C066	GND	;24	E017	Wait	;03
C067	DiskReadData+	;24	E022	K0Data->	;12
C068	DiskReadData-	;24	E024	DCtlFifo->	;06
C069	GND	;24	E025	DBorder->	;05
C070	GND	;24	E032	←KIData'	;13
C201	GND	;24	E041	X.0	;10
C202	ReduceIW'	;24	E042	X.2	;10
C203	GND	;24	E043	X.4	;10
C204	RawSA1/SA4'	;24	E044	X.6	;10
C205	GND	;24	E045	X.8	;10
C206	Sector'	;24	E046	X.10	;10
C207	GND	;24	E047	X.12	;10
C208	SeekComplete'	;24	E048	X.14	;10
C209	GND	;24	E049	Y.00	;06
C210	HeadSelect4'	;24	E050	BackVCC	;01
C211	GND	;24	E051	BackVCC	;01
C212	HeadSelect8'	;24	E052	Y.02	;06
C213	GND	;24	E053	Y.04	;06
C214	HeadSelect1'	;24	E054	Y.06	;06
C215	GND	;24	E055	Y.08	;06
C216	HeadSelect16'	;24	E056	Y.10	;06
C217	GND	;24	E057	Y.12	;06
C218	HeadSelect2'	;24	E058	Y.14	;06
C219	GND	;24	E066	Disp/Proc.'	;08
C220	Index'	;24	E067	DAddr.00	;06
C221	GND	;24	E068	DAddr.02	;06
C222	Ready'	;24	E069	DAddr.04	;06

E071	DAddr.06	:06	E182	DData.11	;05
E072	DAddr.08	:06	E183	DData.13	;05
E073	DAddr.10	:07	E184	DData.15	;05
E074	DAddr.12	:07	E185	ClrDPReq'	;04
E075	DAddr.14	:07	E187	ClrKFlags'	;14
E076	DData.00	:05	E200	BackVEE	;01
E077	DData.02	:05			
E078	DData.04	:05			
E079	DData.06	:05	51MHz': u73.1o	;02	
E081	DData.08	:05	51MHz': u89.9i	;02	
E082	DData.10	:05	51MHz': v06.11i	;08	
E083	DData.12	:05	51MHz': v08.6i	;11	
E084	DData.14	:05			
E085	DPReq'	:04	51MHz: u74.13i	;02	
E087	KReq'	:14	51MHz: u28.9i	;02	
E089	GND	:03	51MHz: u73.3o	;02	
E100	BackVEE	:01	51MHz: v07.9i	;02	
E102	Click.0	:03	51MHz: u56.4i	;04	
E103	Click.1	:03	51MHz: u42.4i	;04	
E104	Click.2	:03	51MHz: u13.13i	;04	
E105	LRAS'	:08	51MHz: u14.9i	;04	
E106	LCAS	:08	51MHz: u57.9i	;08	
E117	IOPReset'	:04	51MHz: u90.9i	;08	
E122	KCtl<'	:12	51MHz: v06.6i	;08	
E124	DCtl<'	:04	51MHz: v26.9i	;08	
E132	←KStatus'	:13	51MHz: v25.13i	;08	
E135	PrinterReq'	:04	51MHz: v08.9o	;11	
E137	EndLine'	:03	51MHz: u29.14o	;11	
E141	X.1	:10			
E142	X.3	:10	A63Ct': u96.9i, u97.8o	;07	
E143	X.5	:10			
E144	X.7	:10	A63Ct: #TP035.1i, u96.15o, u97.9i	;07	
E145	X.9	:10	A63Ct: u62.6i	;07	
E146	X.11	:10	A63Ct: u63.13i	;07	
E147	X.13	:10			
E148	X.15	:10	AbortWrite': u60.1o, u02.4i	;18	
E149	Y.01	:06			
E150	BackVCC	:01	AddrMkFound: u38.3i	;16	
E151	BackVCC	:01	AddrMkFound: u25.17i, u23.17i	;22	
E152	Y.03	:06	AddrMkFound: u39.5o	;22	
E153	Y.05	:06			
E154	Y.07	:06	AdrMkCnt.0: u25.1i, u23.1i	;22	
E155	Y.09	:06	AdrMkCnt.0: #TP099.1i, u24.9o	;22	
E156	Y.11	:06			
E157	Y.13	:06	AdrMkCnt.1: u25.2i, u23.2i	;22	
E158	Y.15	:06	AdrMkCnt.1: #TP100.1i, u24.12o	;22	
E167	DAddr.01	:06			
E168	DAddr.03	:06	AdrMkCnt.2: u25.3i, u23.3i	;22	
E169	DAddr.05	:06	AdrMkCnt.2: #TP101.1i, u24.15o	;22	
E171	DAddr.07	:06	AdrMkCnt.2: u22.13i	;23	
E172	DAddr.09	:06			
E173	DAddr.11	:07	AdrMkCnt.3: u25.4i, u23.4i	;22	
E174	DAddr.13	:07	AdrMkCnt.3: #TP102.1i, u24.16o	;22	
E175	DAddr.15	:07			
E176	DData.01	:05	AdrMkCnt.4: u21.11i	;21	
E177	DData.03	:05	AdrMkCnt.4: u25.7i, u23.7i	;22	
E178	DData.05	:05	AdrMkCnt.4: #TP103.1i, u24.19o	;22	
E179	DData.07	:05			
E181	DData.09	:05	BackVCC: E150, E51, E151, E50	;01	

BackVCC: #F2.2i
 BackVEE: E200, E100, #F1.2i ;01
 BDD.00: v30.2o, v15.4i ;05
 BDD.01: v30.5o, v15.5i ;05
 BDD.02: v30.6o, v15.6i ;05
 BDD.03: v30.9o, v15.7i ;05
 BDD.04: v30.12o, v15.8i ;05
 BDD.05: v30.15o, v12.4i ;05
 BDD.06: v30.16o, v12.5i ;05
 BDD.07: v30.19o, v12.6i ;05
 BDD.08: v29.2o, v14.4i ;05
 BDD.09: v29.5o, v14.5i ;05
 BDD.10: v29.6o, v14.6i ;05
 BDD.11: v29.9o, v14.7i ;05
 BDD.12: v29.12o, v14.8i ;05
 BDD.13: v29.15o, v11.4i ;05
 BDD.14: v29.16o, v11.5i ;05
 BDD.15: v29.19o, v11.6i ;05
 BDrvSelect: #R38.1o, #CR6.1i ;25
 BHoriz: u88.4o ;04
 BHoriz: #L1.2i ;09
 BHoriz: v03.13i ;13
 BitCount.0: u46.15i ;14
 BitCount.0: u37.16i, u36.16i ;16
 BitCount.0: #TP072.1i, u38.5o ;16
 BitCount.1: u46.16i ;14
 BitCount.1: u37.17i, u36.17i ;16
 BitCount.1: #TP073.1i, u38.6o ;16
 BitCount.2: u46.17i ;14
 BitCount.2: u37.1i, u36.1i ;16
 BitCount.2: #TP074.1i, u38.9o ;16
 BitCount.3: u46.1i ;14
 BitCount.3: u37.2i, u36.2i ;16
 BitCount.3: #TP075.1i, u38.12o ;16
 BitMisMatch: u45.6o, u35.12i ;15
 BitVerifyErr': u35.10i, u35.8o ;15
 BitVerifyErr: u47.3i ;14
 BitVerifyErr: u35.9o ;15
 Blank': u73.12o ;04
 Blank': u14.10i ;04
 Blank': u29.15o ;11
 Blk: u79.5i ;04
 Blk: v17.16o, #TP019.1i ;04
 BMFMWriteData: #TP088.1i, u16.5o ;17
 BMFMWriteData: u17.3i ;18
 BNRZWriteData: u59.7o ;15
 BNRZWriteData: u49.14i ;17
 BNRZWriteData: u17.2i ;18
 BPBS: u82.2i, u99.14i, u82.6o ;04
 BpCycle.3: #TP004.1i, v41.10i ;03
 BpCycle.3: v41.7i, v43.5o, v47.12i
 BPumpBias: u40.2i, #R36.1o ;26
 BPumpBias: #C32.1i
 BTransferEnable: v37.1i, v20.1i ;12
 BTransferEnable: #TP048.1i, u87.9o ;12
 BTransferEnable: u50.1i ;12
 BTransferEnable: u68.9i ;14
 BTransferEnable: v21.14i ;15
 BTransferEnable: v38.14i ;15
 BTransferEnable: u02.2i ;18
 BTransferEnable: u08.1i ;22
 BufDCError: #C28.1i, #R30.1o ;25
 BufDCError: #CR5.1o, #C29.1i
 BufX.0: v35.18o ;10
 BufX.0: v36.3i ;12
 BufX.0: v37.3i ;12
 BufX.10: v17.7i ;04
 BufX.10: v18.14o ;10
 BufX.10: v19.7i ;12
 BufX.10: v20.7i ;12
 BufX.11: v17.8i ;04
 BufX.11: v18.12o ;10
 BufX.11: u87.12i ;12
 BufX.11: v20.8i ;12
 BufX.12: v17.13i ;04
 BufX.12: v18.3o ;10
 BufX.12: v19.13i ;12
 BufX.12: v20.13i ;12

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BufX.13: v17.14i ;04
BufX.13: v18.5o ;10
BufX.13: v19.14i ;12
BufX.13: v20.14i ;12

BufX.14: v17.17i ;04
BufX.14: v18.7o ;10
BufX.14: v19.17i ;12
BufX.14: v20.17i ;12

BufX.15: v17.18i ;04
BufX.15: v18.9o ;10
BufX.15: v19.18i ;12
BufX.15: v20.18i ;12

BufX.1: v35.16o ;10
BufX.1: v36.4i ;12
BufX.1: v37.4i ;12

BufX.2: v35.14o ;10
BufX.2: v36.7i ;12
BufX.2: v37.7i ;12

BufX.3: v35.12o ;10
BufX.3: v37.8i ;12
BufX.3: v36.8i ;12

BufX.4: v35.3o ;10
BufX.4: v36.13i ;12
BufX.4: v37.13i ;12

BufX.5: v35.5o ;10
BufX.5: v36.14i ;12
BufX.5: v37.14i ;12

BufX.6: v35.7o ;10
BufX.6: v36.17i ;12
BufX.6: v37.17i ;12

BufX.7: v35.9o ;10
BufX.7: v36.18i ;12
BufX.7: v37.18i ;12

BufX.8: v17.3i ;04
BufX.8: v18.18o ;10
BufX.8: v19.3i ;12
BufX.8: v20.3i ;12

BufX.9: v17.4i ;04
BufX.9: v18.16o ;10
BufX.9: v19.4i ;12
BufX.9: v20.4i ;12

BVert': u88.6o ;04
BVert': #L2.2i ;09
BVert': v05.8i ;13

BWriteEnable: #TP049.1i, u03.10o ;12
BWriteEnable: u46.3i ;14

BWriteEnable: u47.8i ;14
BWriteEnable: u37.6i, u36.6i ;16
BWriteEnable: u49.1i, u31.1i ;17
BWriteEnable: u60.8i ;21

ByteCk: u12.13o ;04
ByteCk: u70.9i ;04

ByteSel: u12.12o ;04
ByteSel: u99.2i ;04

CalibOrData: u59.9o, u21.5i ;21

CAS: v47.3o, E6 ;02

Click.0: v43.14o, E102 ;03
Click.1: v43.12o, E103 ;03
Click.2: v43.3o, E104 ;03

C1k0: #R31.1o, #Q5.2i ;25
C1k1: #R35.1i, #Q5.1i, u53.5i ;25
C1k2: #R29.2i, u53.6o ;25
C1k2: u53.9i ;25
C1k3: #C26.1i, #L3.1o, #R29.1i ;25
C1k4: #R31.2i, #C41.2i, #CR6.2o ;25
C1k4: #L3.2i

C1k: u80.2i, u77.2i, u84.12o ;03
C1k: u98.11i ;14

C1kAdj0: #C43.2i, #R6.2i, #R19.3i ;25
C1kAdj1: #R33.1i, #R19.1i ;25
C1kAdj2: #R19.2o, #R32.2i ;25
C1kAdj3: #CR5.2i, #R32.1o, #C41.1i ;25

C1kSupply: #C27.1i, #Q5.3i ;25
C1kSupply: #C30.1o, #L4.2i

ClockArrived': u26.8o ;19
ClockArrived': #R13.2i, #R15.2i ;26

ClockArrived: #TP122.1i, u53.2i ;19
ClockArrived: u26.9o
ClockArrived: #R12.2i, #R11.2i ;26

ClrCtlFifo': v17.5o ;04
ClrCtlFifo': v32.18i, v13.18i ;06
ClrCtlFifo': v27.18i, v31.18i

ClrDataFifo': u81.15o ;04

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ClrDataFifo': u82.3i ;04
ClrDataFifo': v14.18i, v12.18i ;05
ClrDataFifo': v15.18i, v11.18i
ClrDataFifo': u63.1i ;07

ClrDPReq': E185, u98.13i ;04

ClrKFlags': E187, u98.8i ;14

CompareEnable: u19.9o, u26.12i ;19
CompareEnable: u26.2i

CountReset': u57.6i ;08
CountReset': u92.9o ;08
CountReset': u44.4i ;08
CountReset': u43.13o ;11

CRCData: #TP061.1i, u48.12o ;15
CRCData: u59.3i, u59.4i

CRCError: v04.13i ;13
CRCError: u66.6o ;14

CRCInput: #TP060.1i, u21.4o ;15
CRCInput: u48.11i
CRCInput: u37.5i, u36.5i ;16

Ct.0: v25.14o ;08
Ct.0: u44.6i ;08
Ct.0: u43.11o ;11

Ct.1: v25.15o ;08
Ct.1: u92.5i ;08
Ct.1: u91.5i ;11

Ct.2: v25.2o ;08
Ct.2: u92.7i ;08
Ct.2: u91.13o ;11

Cycle.1': v43.18o, E2 ;03
Cycle.2': v43.16o, E3 ;03

Cycle.3': u73.5i ;02
Cycle.3': v42.9i, v46.1o, E4 ;03

DAddr.00: v32.15o, E67 ;06
DAddr.01: v32.14o, E167 ;06
DAddr.02: v32.13o, E68 ;06
DAddr.03: v32.12o, E168 ;06
DAddr.04: v32.11o, E69 ;06
DAddr.05: v31.15o, E169 ;06
DAddr.06: v31.14o, E71 ;06

DAddr.07: v31.13o, E171 ;06
DAddr.08: v31.12o, E72 ;06
DAddr.09: v31.11o, E172 ;06
DAddr.10: v28.15i, u96.12o, E73 ;07
DAddr.11: v28.13i, u96.13o, E173 ;07
DAddr.12: v28.12i, u96.14o, E74 ;07
DAddr.13: v10.15i, u95.12o, E174 ;07
DAddr.14: v10.13i, u95.13o, E75 ;07
DAddr.15: v10.12i, u95.14o, E175 ;07

DataReq: u34.19o ;14
DataReq: u68.14i, u68.15i ;14

DBorder-': E25, u97.3i ;05
DBorder-': u97.4o, u85.10i ;05

DByte.0: u56.12i ;04
DByte.0: u55.2o ;05
DByte.0: u58.3i ;11

DByte.1: u56.11i ;04
DByte.1: u55.1o ;05
DByte.1: u58.4i ;11

DByte.2: u56.9i ;04
DByte.2: u55.15o ;05
DByte.2: u58.7i ;11

DByte.3: u56.6i ;04
DByte.3: u55.14o ;05
DByte.3: u58.6i ;11

DByte.4: u42.12i ;04
DByte.4: u41.2o ;05
DByte.4: u43.4i ;11

DByte.5: u42.11i ;04
DByte.5: u41.1o ;05
DByte.5: u43.5i ;11

DByte.6: u42.9i ;04
DByte.6: u41.15o ;05
DByte.6: u43.7i ;11

DByte.7: u42.6i ;04
DByte.7: u41.14o ;05
DByte.7: u43.6i ;11

DCAS': v30.11i, v29.11i ;05

```

DCAS': u96.2i, u95.2i ;07
 DCAS': u61.2i, u63.9i ;07
 DCAS': v47.8o ;08

 DCASDly': v15.1i, v15.19i, v12.1i ;05
 DCASDly': v12.19i, v14.1i, v14.19i
 DCASDly': v11.1i, v11.19i
 DCASDly': v23.12o ;08

 DCError: #R30.2i ;25
 DCError: #C40.1i, #Q4.3i, #Q1.3i ;26

 DCF.00: v34.2o, v27.8i ;06

 DCF.01: v34.5o, v13.4i ;06

 DCF.02: v34.6o, v13.5i ;06

 DCF.03: v34.9o, v13.6i ;06

 DCF.04: v34.12o, v13.7i ;06

 DCF.05: v34.15o, v13.8i ;06

 DCF.06: v34.16o, v32.4i ;06

 DCF.07: v34.19o, v32.5i ;06

 DCF.08: v33.2o, v32.6i ;06

 DCF.09: v33.5o, v32.7i ;06

 DCF.10: v33.6o, v32.8i ;06

 DCF.11: v33.9o, v31.4i ;06

 DCF.12: v33.12o, v31.5i ;06

 DCF.13: v33.15o, v31.6i ;06

 DCF.14: v33.16o, v31.7i ;06

 DCF.15: v33.19o, v31.8i ;06

 DCt1Fifo<': E24, u97.1i ;06

 DCt1Fifo<: u97.2o, u85.5i ;06

 DCt1<': E124, u97.5i ;04

 DCt1<: u97.6o, u85.2i ;04

 DData.00: E76, v30.3i ;05

 DData.01: E176, v30.4i ;05

 DData.02: E77, v30.7i ;05

 DData.03: E177, v30.8i ;05

 DData.04: E78, v30.13i ;05

 DData.05: E178, v30.14i ;05

 DData.06: E79, v30.17i ;05

 DData.07: E179, v30.18i ;05

 DData.08: E81, v29.3i ;05

 DData.09: E181, v29.4i ;05

 DData.10: E82, v29.7i ;05

 DData.11: E182, v29.8i ;05

 DData.12: E83, v29.13i ;05

 DData.13: E183, v29.14i ;05

 DData.14: E84, v29.17i ;05

 DData.15: E184, v29.18i ;05

 DelInputData: u26.3i, u54.8o ;19
 DelInputData: u09.3i ;21

 DelTransferEnb: u50.6o ;12
 DelTransferEnb: u34.1i ;14
 DelTransferEnb: u38.1i, u52.1i ;16

 DelVerifyError: u66.16o ;14
 DelVerifyError: u66.4i ;14

 DirectionIn': v03.15i ;13
 DirectionIn': u07.6o ;18
 DirectionIn': C234 ;24

 DirectionIn: v19.5o ;12
 DirectionIn: u07.5i ;18

 DisableMFMC1k': u53.4i ;25
 DisableMFMC1k': #TP120.1i, u65.12o ;27

 DiskOutputClk+: u10.12i, u10.13o ;18
 DiskOutputClk+: C59 ;24

 DiskOutputClk-: u10.15i, u10.14o ;18
 DiskOutputClk-: C60 ;24

 DiskOutputClk: v03.6i ;13
 DiskOutputClk: u10.9i ;18
 DiskOutputClk: u22.7o ;23

 DiskReadClk+: u11.1i ;20
 DiskReadClk+: C55 ;24
 DiskReadClk+: #R2.1i ;24

DiskReadClk-: u11.2i ;20
 DiskReadClk-: C56 ;24
 DiskReadClk-: #R3.1i ;24

 DiskReadClk: v03.2i ;13
 DiskReadClk: u11.4o ;20
 DiskReadClk: u08.11i ;21
 DiskReadClk: u22.5i ;23
 DiskReadClk: u22.11i ;23

 DiskReadData+: u11.12i ;20
 DiskReadData+: C67 ;24
 DiskReadData+: #R4.1i ;24

 DiskReadData-: u11.11i ;20
 DiskReadData-: C68 ;24
 DiskReadData-: #R5.1i ;24

 DiskReadData: v03.4i ;13
 DiskReadData: u11.9o ;20
 DiskReadData: u59.13i, u59.11i ;21

 DiskWriteData+: u10.4i, u10.3o ;18
 DiskWriteData+: C63 ;24

 DiskWriteData-: u10.1i, u10.2o ;18
 DiskWriteData-: C64 ;24

 DiskWriteData: v03.8i ;13
 DiskWriteData: u10.5i, u17.4o ;18
 DiskWriteData: u21.6i ;21

 Disp/Proc.': v47.9i, v23.13o, E66 ;08

 DispReq': u86.12i ;04
 DispReq': u69.3o ;04

 DPReq': u98.6o, E85 ;04

 DProm.00: u80.11o ;03
 DProm.00: u78.15i, u79.15i ;04

 DProm.01: u80.12o ;03
 DProm.01: u78.16i, u79.16i ;04

 DProm.02: u80.13o ;03
 DProm.02: u78.17i, u79.17i ;04

 DProm.03: u80.14o ;03
 DProm.03: u78.1i, u79.1i ;04

 DProm.04: u77.11o ;03
 DProm.04: u78.2i, u79.2i ;04

 DProm.05: u77.12o ;03
 DProm.05: u78.3i, u79.3i ;04

 DProm.06: u77.13o ;03
 DProm.06: u78.4i, u79.4i ;04

 DProm.07: u77.14o ;03
 DProm.07: u78.7i, u79.7i ;04

 DriveNotReady: v04.8i ;13
 DriveNotReady: u20.4o ;20

 DriveSelect': v05.6i ;13
 DriveSelect': u07.12o ;18
 DriveSelect': C226 ;24

 DriveSelect: v36.15o ;12
 DriveSelect: u07.13i ;18
 DriveSelect: u67.3i ;23
 DriveSelect: #R38.2i ;25

 DrvMFMClock': u26.11i ;19
 DrvMFMClock': u53.11o ;25

 DrvMFMClock: u09.11i ;21
 DrvMFMClock: u08.3i, u39.3i ;22
 DrvMFMClock: u24.11i
 DrvMFMClock: u53.13i, #TP107.1i ;25
 DrvMFMClock: u53.8o, u53.12i

 DWE1: u47.13i ;14
 DWE1: u47.9o ;14

 DWE2: u47.14i ;14
 DWE2: u47.12o ;14

 DWE3: u47.15o ;14
 DWE3: u47.17i ;14

 DWE4: u47.18i ;14
 DWE4: u47.16o ;14

 DWriteEnable: u47.19o ;14
 DWriteEnable: u02.5i ;18
 DWriteEnable: u60.9i ;21

 ECL1: u76.15o ;02
 ECL1: u74.7i, u74.11i ;02
 ECL1: v25.7i ;08
 ECL1: u91.3i ;11

 ECLCAS': v24.3i ;02
 ECLCAS': u89.2o ;02
 ECLCAS': v08.7i ;11

 ECLCycle3': u73.2o ;02
 ECLCycle3': v07.10i ;02
 ECLCycle3': u30.5i ;08
 ECLCycle3': u29.12o ;11

 ECLppClk': u89.14o ;02
 ECLppClk': v24.15i ;02
 ECLppClk': v08.11o ;11

ECLRAS': u28.5i ;02
 ECLRAS': v24.10i ;02
 ECLRAS': u89.5i ;02
 ECLRAS': v07.3o ;02
 ECLRAS': u29.4i ;11

 ECLWPulse: v24.7i ;02
 ECLWPulse: u74.15o ;02
 ECLWPulse: u76.7i ;02
 ECLWPulse: u91.4i ;11

 ECt.0: u62.15i ;07
 ECt.0: #TP044.1i, u63.2o ;07

 ECt.1: u62.1i ;07
 ECt.1: #TP045.1i, u63.7o ;07

 ECt.2: u62.2i ;07
 ECt.2: #TP046.1i, u63.10o ;07

 Enb51MHz: u72.2i ;02
 Enb51MHz: #TP112.1i, u65.15o ;10

 EnbDBorder: v16.11i, v01.11i ;05
 EnbDBorder: u85.8o

 EnbDCtl: u85.3o, v17.11i ;04

 EnbDCtlFifo: v31.1i, v32.19i ;06
 EnbDCtlFifo: v32.1i, v13.19i
 EnbDCtlFifo: v13.1i, v27.19i
 EnbDCtlFifo: v27.1i, u85.6o
 EnbDCtlFifo: v31.19i

 EndAddr.10: #TP028.1i, v27.11o ;06
 EndAddr.10: v28.1i ;07

 EndAddr.11: #TP029.1i, v13.15o ;06
 EndAddr.11: v28.14i ;07

 EndAddr.12: #TP030.1i, v13.14o ;06
 EndAddr.12: v28.11i ;07

 EndAddr.13: #TP031.1i, v13.13o ;06
 EndAddr.13: v10.1i ;07

 EndAddr.14: #TP032.1i, v13.12o ;06
 EndAddr.14: v10.14i ;07

 EndAddr.15: #TP033.1i, v13.11o ;06
 EndAddr.15: v10.11i ;07

 EndLine': u80.9i, v41.1i, u77.9i ;03
 EndLine': u88.2o, E137

 EndLine: u88.1i, u80.15o, v46.3i ;03
 EndLine: u27.11i ;04

 EndRndRead': #TP040.1i, u61.1i ;07

EndRndRead': u62.9o
 EndRndRead': u69.10i ;07
 EndRndRead': u27.7i ;08

 EndSeg: u69.13i, #TP034.1i, v28.6o ;07
 EndSeg: v46.12i

 ENRZClock: #TP087.1i, u33.5i ;17
 ENRZClock: u49.19o, u32.5i

 ENRZWriteData: #TP085.1i, u33.7i ;17
 ENRZWriteData: u49.15o, u32.7i

 ESyncWdFound: #TP086.1i, u33.6i ;17
 ESyncWdFound: u49.16o, u32.6i

 F/P': u69.8o ;07
 F/P': u27.10i ;08

 FaultClear': u07.10o ;18
 FaultClear': C232 ;24

 FaultClear: v36.16o ;12
 FaultClear: u07.11i ;18

 FildCError: #C31.1i, #C40.2i ;26
 FildCError: #R37.1i

 FilHSync: #C2.1o, #R9.2i ;09

 FilVSync': #C3.1o, #R10.2i ;09

 FirmwareEnable: v19.6o ;12
 FirmwareEnable: v02.11i ;13
 FirmwareEnable: u68.4i ;14

 Full: u92.15o ;08
 Full: u92.14o ;08
 Full: u90.7i ;08
 Full: u76.11i ;08
 Full: u91.9o ;11

 Gated51MHz': u72.3o ;02
 Gated51MHz': u83.3i, u73.7i ;02
 Gated51MHz': #TP113.1i, #R34.1i ;09

 GND: #C93.2i ;01
 GND: #C92.1i ;01
 GND: u88.11i ;02
 GND: v42.4i ;03
 GND: v41.4i, v41.5i, v41.6i ;03
 GND: v41.3i
 GND: u80.3i, u80.5i, u80.6i ;03
 GND: u77.3i
 GND: v46.6i ;03
 GND: v43.1i ;03
 GND: v43.11i, v43.13i ;03
 GND: E89 ;03
 GND: u82.12i ;04

GND: u81.1i ;04
 GND: u78.6i ;04
 GND: v30.1i ;05
 GND: v29.1i ;05
 GND: v34.1i ;06
 GND: v33.1i ;06
 GND: v32.9i, v31.9i ;06
 GND: u95.4i, u95.3i, u95.5i ;07
 GND: v10.2i, v10.4i, v10.9i ;07
 GND: v10.10i
 GND: v28.2i, v28.4i, v28.9i ;07
 GND: v28.10i
 GND: u96.4i, u96.3i, u96.5i ;07
 GND: #C2.2i ;09
 GND: #C3.2i ;09
 GND: C2 ;09
 GND: C4 ;09
 GND: C9, C7 ;09
 GND: #CR1.1o ;09
 GND: #CR2.1o ;09
 GND: u43.16i, u75.16i, u91.16i ;09
 GND: v08.16i, u29.16i
 GND: v35.1i ;10
 GND: v18.1i ;10
 GND: u68.7i ;14
 GND: u98.1i ;14
 GND: u68.12i, u68.13i ;14
 GND: u48.5i, u48.3i, u48.4i ;15
 GND: u48.8i
 GND: v21.11i ;15
 GND: v38.11i ;15
 GND: u59.15i, u59.1i ;15
 GND: u37.15i, u36.15i ;16
 GND: u16.7i ;17
 GND: u17.15i ;18
 GND: u21.15i ;21
 GND: u25.15i, u23.15i ;22
 GND: u22.15i ;23
 GND: #R4.2o, #R3.2o, #R2.2o ;24
 GND: #R5.2o
 GND: C203, C205, C207, C209, C211 ;24
 GND: C213, C215, C217, C219, C221
 GND: C223, C225, C227, C229, C231
 GND: C233, C235, C237, C239, C241
 GND: C243, C245, C247, C249, C201
 GND: C52, C54, C58, C62, C66, C70 ;24
 GND: C61, C65, C69
 GND: #R33.2i, #C43.1i, #C42.1i ;25
 GND: #C27.2i ;25
 GND: #C30.2i ;25
 GND: #C29.2i, #C28.2i ;25
 GND: #C26.2o ;25
 GND: #C19.2o, #R23.1o ;26
 GND: #C23.2o, #R22.1o ;26
 GND: #C24.2i ;26
 GND: #R37.2i, #C31.2i ;26
 GND: #C25.2i ;26
 GND: #R27.2i ;26
 GND: u40.3i ;26

GND: #C91.2o, #C90.2o, #C89.2o ;28
 GND: #C88.2o, #C87.2o, #C86.2o
 GND: #C85.2o, #C84.2o, #C83.2o
 GND: #C82.2o, #C81.2o, #C80.2o
 GND: #C79.2o, #C77.2o, #C76.2o
 GND: #C75.2o, #C74.2o, #C73.2o
 GND: #C70.2o, #C69.2o, #C68.2o
 GND: #C67.2o, #C66.2o, #C65.2o
 GND: #C64.2o, #C63.2o, #C60.2o
 GND: #C59.2o, #C58.2o, #C57.2o
 GND: #C56.2o, #C52.2o, #C51.2o
 GND: #C50.2o, #C49.2o, #C48.2o
 GND: #C47.2o, #C46.2o, #C39.2o
 GND: #C38.2o, #C37.2o, #C36.2o
 GND: #C18.2o, #C17.2o, #C16.2o
 GND: #C15.2o, #C14.2o, #C13.2o
 GND: #C12.2o, #C9.2o, #C8.2o
 GND: #C7.2o, #C6.2o, #C5.2o
 GND: #C4.2o, #C78.2o, #C72.2o
 GND: #C71.2o, #C62.2o, #C61.2o
 GND: #C55.2o, #C54.2o, #C53.2o
 GND: #C45.2o, #C44.2o, #C35.2o
 GND: #C34.2o, #C33.2o, #C22.2o
 GND: #C21.2o, #C20.2o, #C11.2o
 GND: #C10.2o, #C1.2o

 HalfClk: u83.2i, u83.6o ;02
 HalfClk: v00.3i, v00.11i ;21

 HeadSelect1': v02.17i ;13
 HeadSelect1': u04.2o ;18
 HeadSelect1': C214 ;24

 HeadSelect16': v02.2i ;13
 HeadSelect16': u07.2o ;18
 HeadSelect16': C216 ;24

 HeadSelect16: v36.2o ;12
 HeadSelect16: u07.1i ;18

 HeadSelect1: v36.12o ;12
 HeadSelect1: u04.1i ;18

 HeadSelect2': v02.8i ;13
 HeadSelect2': u04.4o ;18
 HeadSelect2': C218 ;24

 HeadSelect2: v36.9o ;12
 HeadSelect2: u04.3i ;18

 HeadSelect4': v02.6i ;13
 HeadSelect4': u04.6o ;18
 HeadSelect4': C210 ;24

 HeadSelect4: v36.6o ;12
 HeadSelect4: u04.5i ;18

 HeadSelect8': v02.4i ;13
 HeadSelect8': u04.8o ;18

HeadSelect8': C212 ;24
 HeadSelect8: v36.5o ;12
 HeadSelect8: u04.9i ;18
 HighBorderOut: #TP008.1i, u99.11o ;04
 HighBorderOut: v01.1i ;05
 HighDataOut: #TP006.1i, u99.6o ;04
 HighDataOut: v15.9i, v12.9i ;05
 Horiz': u88.3i ;04
 Horiz': u70.10o ;04
 HSync: #R9.1o, #L1.1o, C1 ;09
 Index': u05.11i ;20
 Index': u18.3i ;20
 Index': C220 ;24
 Index: u05.10o ;20
 Index: u87.3i ;23
 IndexFound: v04.2i ;13
 IndexFound: u68.2i ;14
 IndexFound: u87.5o ;23
 InhibitRead': u97.12o ;07
 InhibitRead': u27.6i ;08
 InhibitRead: u63.15o, u97.13i ;07
 InpPlsD10': u19.1i, u03.12o ;19
 InpPlsD10: u54.12o, u03.13i ;19
 InputArrived': u26.6o ;19
 InputArrived': #R16.2i ;26
 InputArrived: #TP121.1i, u53.1i ;19
 InputArrived: u26.5o
 InputArrived: #R14.2i ;26
 InputData: u19.3i ;19
 InputData: u19.11i ;19
 InputData: #TP089.1i, u08.12i ;21
 InputData: u21.7o
 InputPulse: u19.5o, u54.1i ;19
 InrHiPrAddr: u80.10i, u80.7i ;03
 InrHiPrAddr: u77.15o
 Invert: u73.11i ;04
 Invert: v17.12o ;04
 IOPReset': E117, v17.1i ;04
 IOPReset': v19.1i, v36.1i, u87.13i ;12
 IOPReset': u03.3i ;18

IOPReset: u03.4o, u60.3i ;18
 KCtlC1k: v19.11i, u87.11i, u86.3o ;12
 KCtlC1k: v36.11i
 KCtl': E122, u84.1i ;12
 KCtl': u67.2i ;14
 KCtl': u84.2o, u86.2i ;12
 KOData': E22, u84.3i ;12
 KOData': u67.13i ;14
 KOData': u84.4o, u86.5i ;12
 KReq': u98.5o, E87 ;14
 LastTick': u76.5i ;08
 LastTick': v25.4o ;08
 LastTick': u92.10i ;08
 LastTick': v26.11i ;08
 LastTick': u44.5i ;08
 LastTick': u44.7i ;08
 LastTick': u43.10o ;11
 LCAS: v47.10i, v45.6o, E106 ;08
 LdSR': u56.7i, u42.7i ;04
 LdSR': v26.15o ;04
 LdSR': u14.11i ;04
 LdSR': u29.11o ;11
 LdWrd': u12.6i ;04
 LdWrd': u13.4o ;04
 LdWrd': u29.13o ;11
 LdWrd: u12.5o ;04
 LdWrd: u69.5i ;04
 LoAdrEqual: v28.3i, v10.6o ;07
 LoDAdrCarry': u95.9i, u97.10o ;07
 LoDAdrCarry: #TP036.1i, u97.11i ;07
 LoDAdrCarry: u95.15o, u96.10i
 LoDAdrCarry: u96.7i, v46.11i
 LowBorderOut: #TP009.1i, u99.12o ;04
 LowBorderOut: v16.1i ;05
 LowDataOut: #TP007.1i, u99.7o ;04
 LowDataOut: v14.9i, v11.9i ;05
 LRAS': v45.3o, E105 ;08
 MFMDetected.0: u24.4i, u24.2o ;22
 MFMDetected.0: u25.6i, u23.6i ;22

MFMDetected.1: #TP098.1i, u24.5o ;22
 MFMDetected.1: u25.5i, u23.5i ;22
 MFMWr20: u01.4o, u16.15i ;17
 MFMWr30: u16.1i, u16.2i, u16.3i ;17
 MFMWr30: u16.4i, u01.10o, u16.14i
 MFMWr40: u16.12i, u01.6o, u16.13i ;17
 NRZClock': v39.11i, v22.11i ;13
 NRZClock': u47.11i ;14
 NRZClock': u48.1i ;15
 NRZClock': u84.8o ;23
 NRZClock: u50.11i ;12
 NRZClock: u34.11i ;14
 NRZClock: v21.13i ;15
 NRZClock: v38.13i ;15
 NRZClock: u35.11i ;15
 NRZClock: u38.11i, u52.3i ;16
 NRZClock: u49.18i ;17
 NRZClock: u84.9i, u22.9o ;23
 NRZInput: u45.5i ;15
 NRZInput: v21.1i, v21.2i ;15
 NRZInput: u21.2i ;15
 NRZInput: u22.12o ;23
 NRZpWrData.0: u33.15i, u32.15i ;17
 NRZpWrData.0: u31.2o
 NRZpWrData.1: u33.1i, u32.1i ;17
 NRZpWrData.1: u31.5o
 NRZpWrData.2: u33.2i, u32.2i ;17
 NRZpWrData.2: u31.6o
 NRZpWrData.3: u33.3i, u32.3i ;17
 NRZpWrData.3: u31.9o
 NRZpWrData.4: u33.4i, u32.4i ;17
 NRZpWrData.4: u31.12o
 Odd: u78.5i ;04
 Odd: v17.9o ;04
 On: v17.19o ;04
 On: u69.1i ;04
 One16thRef: u06.6o, u06.13i ;23
 Overrun: v04.15i ;13
 Overrun: u66.19o ;14
 PAddrMkFound: #TP097.1i, u25.14o ;22
 PAddrMkFound: u39.2i
 PAddrMkCnt.0: #TP092.1i, u23.13o ;22
 PAddrMkCnt.0: u24.8i
 PAddrMkCnt.1: #TP093.1i, u23.14o ;22
 PAddrMkCnt.1: u24.13i
 PAddrMkCnt.2: #TP094.1i, u25.11o ;22
 PAddrMkCnt.2: u24.14i
 PAddrMkCnt.3: #TP095.1i, u25.12o ;22
 PAddrMkCnt.3: u24.17i
 PAddrMkCnt.4: #TP096.1i, u25.13o ;22
 PAddrMkCnt.4: u24.18i
 Page/Full': u69.9i, v46.13o ;07
 Page/Full': u62.5i ;07
 PBitCount.0: #TP064.1i, u36.12o ;16
 PBitCount.0: u38.4i
 PBitCount.1: #TP065.1i, u36.13o ;16
 PBitCount.1: u38.7i
 PBitCount.2: #TP066.1i, u36.14o ;16
 PBitCount.2: u38.8i
 PBitCount.3: #TP067.1i, u37.11o ;16
 PBitCount.3: u38.13i
 PB1k: u81.5o ;04
 PB1k: u70.13i ;04
 PB1kSync: u73.10i ;04
 PB1kSync: u70.15o ;04
 pCAS: v47.2i, v47.1i, v24.4o ;02
 pCDFifo: #TP015.1i, u78.12o ;04
 pCDFifo: u81.14i
 pClick.0: v47.13i, v41.12o, v43.6i ;03
 pClick.1: v41.13o, v43.8i ;03
 pClick.2: v41.14o, v43.17i ;03
 PCt.0: #TP041.1i, u62.10o, u63.4i ;07
 PCt.1: #TP042.1i, u62.11o, u63.5i ;07
 PCt.2: #TP043.1i, u62.12o, u63.12i ;07
 pCycle.1': v42.14o, v43.4i ;03
 pCycle.2': v42.13o, v43.2i ;03
 pCycle.3: v43.15i, v42.15o, v46.2i ;03
 PD/P: u81.6o ;04

PD/P: u27.5i ;08
 pDispReq: u82.8o, u69.2i ;04
 pDPReq': u86.8o, u98.7i ;04
 pDPReq: u86.9i, u86.11o, u86.10i ;04
 PHoriz': u81.2o ;04
 PHoriz': u70.12i ;04
 Pic: u79.6i ;04
 Pic: v17.15o, #TP018.1i ;04
 pKReq': u98.2o, u98.4i ;14
 pLCAS: v45.5i, v45.4i, v23.4o ;08
 PLdSerialNRZ': v21.23i ;15
 PLdSerialNRZ': v38.23i ;15
 PLdSerialNRZ': u38.16o ;16
 pLRAS: v45.2i, v45.1i, v23.5o ;08
 pNil: #TP017.1i, u78.14o, u81.18i ;04
 PNRZpWrData.0: #TP077.1i, u33.9o ;17
 PNRZpWrData.0: u31.3i
 PNRZpWrData.1: #TP078.1i, u33.10o ;17
 PNRZpWrData.1: u31.4i
 PNRZpWrData.2: #TP079.1i, u33.11o ;17
 PNRZpWrData.2: u31.7i
 PNRZpWrData.3: #TP080.1i, u33.12o ;17
 PNRZpWrData.3: u31.8i
 PNRZpWrData.4: #TP081.1i, u32.9o ;17
 PNRZpWrData.4: u31.13i
 pPB1k: #TP011.1i, u79.12o, u81.4i ;04
 ppClk: v45.11o, v45.8o, E9 ;02
 ppClk: v46.8i, v46.5i ;03
 ppClk: v42.2i ;03
 ppClk: v41.2i ;03
 pPD/P: #TP012.1i, u79.13o, u81.7i ;04
 pPHoriz': #TP010.1i, u79.11o ;04
 pPHoriz': u81.3i
 PPic: u81.9o ;04
 PPic: u70.4i ;04
 PPicSync: u99.13i, u99.3i ;04
 PPicSync: u70.2o, #TP005.1i ;04
 PPicSync: u70.5i ;04
 PPicSyncDly: u69.4i ;04
 PPicSyncDly: u70.7o ;04
 PPLC: u44.3o ;08
 PPLC: u90.10i ;08
 PPLC: u91.2i ;11
 PPLdSerialNRZ': #TP069.1i, u37.13o ;16
 PPLdSerialNRZ': u38.17i
 pppClk': v45.9i, v45.13i, v45.12i ;02
 pppClk': v24.13o, v45.10i
 pPPic: #TP013.1i, u79.14o, u81.8i ;04
 PPRawOverrun: #TP053.1i, u46.13o ;14
 PPRawOverrun: u34.17i
 PPreComp.0: #TP083.1i, u32.11o ;17
 PPreComp.0: u31.17i
 PPreComp.1: #TP084.1i, u32.12o ;17
 PPreComp.1: u31.18i
 pPReq': #TP016.1i, u78.13o ;04
 pPReq': u81.17i
 pRAS: v47.5i, v47.4i, v24.12o ;02
 PRawOverrun: u47.4i ;14
 PRawOverrun: u34.16o ;14
 PReadData.0: v39.2o, v44.3i ;13
 PReadData.10: v22.6o, v40.7i ;13
 PReadData.11: v22.9o, v40.8i ;13
 PReadData.12: v22.12o, v40.13i ;13
 PReadData.13: v22.15o, v40.14i ;13
 PReadData.14: v22.16o, v40.17i ;13
 PReadData.15: v22.19o, v40.18i ;13
 PReadData.1: v39.5o, v44.4i ;13
 PReadData.2: v39.6o, v44.7i ;13
 PReadData.3: v39.9o, v44.8i ;13
 PReadData.4: v39.12o, v44.13i ;13
 PReadData.5: v39.15o, v44.14i ;13
 PReadData.6: v39.16o, v44.17i ;13

PReadData.7: v39.19o, v44.18i ;13
 PReadData.8: v22.2o, v40.3i ;13
 PReadData.9: v22.5o, v40.4i ;13
 preCAS': u28.2o ;02
 preCAS': u28.6i ;02
 preCAS': v09.12i ;08
 preCAS': v08.5i ;11
 preC1k': v46.4o, u84.13i ;03
 preC1k': v34.11i, v33.11i ;06
 PreComp.0: u16.10i ;17
 PreComp.0: u31.16o ;17
 PreComp.1: u16.11i ;17
 PreComp.1: u31.19o ;17
 preDisp/Proc.': v26.3o ;08
 preDisp/Proc.': v23.15i ;08
 preDisp/Proc.': v09.9i ;08
 preDisp/Proc.': v08.10o ;11
 preLCAS': u28.10i ;08
 preLCAS': u90.14o ;08
 preLCAS': v09.13i ;08
 preLCAS': u29.7i ;11
 preLRAS: u90.3o ;08
 preLRAS: v09.11i ;08
 preLRAS: u75.15o ;11
 PReq': u81.16o ;04
 PReq': u82.13i ;04
 PReqState.0: #TP051.1i, u46.11o ;14
 PReqState.0: u34.13i
 PReqState.1: #TP052.1i, u46.12o ;14
 PReqState.1: u34.14i
 preRAS: v07.15o ;02
 preRAS: v07.7i ;02
 preRAS: v09.10i ;08
 preRAS: u91.14o ;11
 preWaitC1k': v46.10o ;03
 preWaitC1k': u85.1i ;04
 preWaitC1k': u85.9i ;05
 preWaitC1k': u85.4i ;06
 preWaitC1k': u86.1i ;12
 preWaitC1k': u86.4i ;12
 preWaitC1k': u67.11i ;14
 PrinterReq': E135, u86.13i ;04
 PrinterReq': u18.9o ;20
 PSA1Sector: #TP091.1i, u23.12o ;22
 PSA1Sector: u24.7i
 PSA4000Req: #TP054.1i, u46.14o ;14
 PSA4000Req: u34.18i
 PSyncWdFound: #TP068.1i, u37.12o ;16
 PSyncWdFound: u38.14i
 PullUp: u88.10o ;02
 PullUp: u73.6i ;02
 PullUp: u83.4i ;02
 PullUp: u77.4i, u77.5i, u77.6i ;03
 PullUp: u80.4i, u77.10i, u77.7i
 PullUp: v42.10i, v42.3i, v42.5i ;03
 PullUp: v42.6i, v42.7i
 PullUp: v43.19i ;03
 PullUp: u82.1i ;04
 PullUp: u82.11i ;04
 PullUp: u83.10i ;04
 PullUp: u83.13i ;04
 PullUp: u70.1i ;04
 PullUp: u55.6i ;05
 PullUp: u41.6i ;05
 PullUp: u96.6i ;07
 PullUp: u61.10i, u61.9i, u61.7i ;07
 PullUp: u95.7i, u95.10i, u95.6i ;07
 PullUp: v10.3i ;07
 PullUp: v35.19i ;10
 PullUp: v18.19i ;10
 PulseTrap': u09.2i, u09.6o ;21
 PulseTrap: u09.5o, u09.12i ;21
 PumpBias: #R27.1o, #Q3.3i, #Q2.3i ;26
 PumpBias: #R36.2i
 PumpDown': #R20.2i, #R15.1o ;26
 PumpDown': #Q3.2i ;26
 PumpDown: #R17.2i, #R11.1o ;26
 PumpDown: #Q4.2i ;26
 PumpDownBias: #R22.2i, #CR4.1o ;26
 PumpDownBias: #R17.1o, #R20.1o
 PumpDownBias: #C23.1i
 PumpDownSupply: #Q4.1i, #Q3.1i ;26
 PumpDownSupply: #R28.1o, #R24.2i
 PumpFeedBack: #R26.1o, #C32.2o ;26
 PumpFeedBack: u40.6o, #R24.1o
 PumpUp': #R18.2i, #R16.1o ;26
 PumpUp': #Q1.2i ;26
 PumpUp: #R21.2i, #R14.1o ;26
 PumpUp: #Q2.2i ;26

PumpUpBias: #R23.2i, #CR3.2i ;26
 PumpUpBias: #R21.1o, #R18.1o
 PumpUpBias: #C19.1i

 PumpUpSupply: #Q1.1i, #Q2.1i ;26
 PumpUpSupply: #R25.1o, #R26.2i

 PUnCompMFM: #TP082.1i, u32.10o ;17
 PUnCompMFM: u31.14i

 pVert: v17.6o, u83.12i ;04

 PVid: u14.14o ;04
 PVid: u14.7i ;04
 PVid: u44.14o ;04
 PVid: u43.1i ;11

 pVtClk: #TP014.1i, u78.11o ;04
 pVtClk: u81.13i

 PWordBoundry': #TP070.1i, u37.14o ;16
 PWordBoundry': u52.2i

 RAS': v47.6o, E5 ;02

 Raw51Mhz: u71.8o, u72.1i ;02

 RawCRCError: u66.7i ;14
 RawCRCError: #TP062.1i, u48.13o ;15

 RawOverrun: u47.5o, u66.18i ;14
 RawOverrun: u60.2i ;18

 RawSA1/SA4': u18.7i ;20
 RawSA1/SA4': u20.9i ;20
 RawSA1/SA4': C204 ;24

 RawVerifyError: u47.2o, u66.17i ;14

 RCE': u90.6i ;08
 RCE': u92.3o, u92.2o ;08
 RCE': u75.7i ;11

 RCtrPE': v25.5i ;08
 RCtrPE': u44.2o ;08
 RCtrPE': u91.15o ;11

 ReadDataFifo: u69.6o ;04
 ReadDataFifo: v15.16i, v12.16i ;05
 ReadDataFifo: v14.16i, v11.16i

 ReadGate': v05.13i ;13
 ReadGate': u02.3o ;18
 ReadGate': C238 ;24

 Ready': u20.1i ;20
 Ready': u18.4i ;20
 Ready': C222 ;24

Ready: u20.2o, u20.3i ;20

 ReduceIW': v03.11i ;13
 ReduceIW': u07.4o ;18
 ReduceIW': C202 ;24

 ReduceIW: v36.19o ;12
 ReduceIW: u16.9i ;17
 ReduceIW: u07.3i ;18

 RefMFMClock': v00.1i, v00.8o ;21

 RefMFMClock: u49.11i, u31.11i ;17
 RefMFMClock: v00.9o ;21
 RefMFMClock: u59.12i, u59.10i ;21
 RefMFMClock: u06.1i ;23

 ReqState.0: #TP055.1i, u34.12o ;14
 ReqState.0: u46.6i ;14

 ReqState.1: u46.5i ;14
 ReqState.1: #TP056.1i, u34.15o ;14

 ResetClick: v41.9i, v47.11o ;03

 ResetCompare': u26.13i, u26.1i ;19
 ResetCompare': u19.13i, u53.3o

 RSeekComplete: u94.12i, u94.2i ;23
 RSeekComplete: u67.6o, #TP106.1i

 SA1000'/SA4000: u20.8o, u20.11i ;20

 SA1000/SA4000': v04.6i ;13
 SA1000/SA4000': u46.2i ;14
 SA1000/SA4000': u17.1i ;18
 SA1000/SA4000': u20.10o ;20
 SA1000/SA4000': u25.16i, u23.16i ;22
 SA1000/SA4000': u22.1i ;23

 SA1NRZClock: u21.9o ;21
 SA1NRZClock: u22.10i ;23

 SA1Sector: u24.6o ;22
 SA1Sector: u22.3i ;23

 SA1SkComplete: u59.14i ;15
 SA1SkComplete: u05.6o ;20
 SA1SkComplete: u67.5i, u17.6i ;23

 SA1WrNRZClock: u21.10i ;21
 SA1WrNRZClock: u06.3o ;23

 SA4Sector: u20.12o ;20
 SA4Sector: u22.2i ;23
 SA4Sector: u60.6i ;23

 SA4SkComplete: u17.5i, u93.11o ;23

SA4SkComplete: #TP105.1i, u60.5i
 SAddrMkFound: #TP071.1i, u38.2o ;16
 SAddrMkFound: u37.4i, u36.4i ;16
 Sector': v05.4i ;13
 Sector': u18.6i ;20
 Sector': u20.13i ;20
 Sector': C206 ;24
 Sector: u22.4o, u39.11i ;23
 SectorFound: v04.4i ;13
 SectorFound: u68.1i ;14
 SectorFound: u39.9o ;23
 SeekComplete': v03.17i ;13
 SeekComplete': u05.5i ;20
 SeekComplete': u18.1i ;20
 SeekComplete': C208 ;24
 SeekComplete: v02.15i ;13
 SeekComplete: u68.3i ;14
 SeekComplete: u17.7o ;23
 SerialNRZ.0: v39.3i ;13
 SerialNRZ.0: #TP059.1i, u59.6i ;15
 SerialNRZ.0: u59.5i, v38.21o
 SerialNRZ.0: u45.4i ;15
 SerialNRZ.0: u21.3i ;15
 SerialNRZ.10: v22.7i ;13
 SerialNRZ.10: v21.17o ;15
 SerialNRZ.11: v22.8i ;13
 SerialNRZ.11: v21.15o ;15
 SerialNRZ.12: v22.13i ;13
 SerialNRZ.12: v21.10o ;15
 SerialNRZ.13: v22.14i ;13
 SerialNRZ.13: v21.8o ;15
 SerialNRZ.14: v22.17i ;13
 SerialNRZ.14: v21.6o ;15
 SerialNRZ.15: v22.18i ;13
 SerialNRZ.15: v21.4o ;15
 SerialNRZ.1: v39.4i ;13
 SerialNRZ.1: v38.19o ;15
 SerialNRZ.2: v39.7i ;13
 SerialNRZ.2: v38.17o ;15
 SerialNRZ.3: v39.8i ;13
 SerialNRZ.3: v38.15o ;15
 SerialNRZ.4: v39.13i ;13
 SerialNRZ.4: v38.10o ;15
 SerialNRZ.5: v39.14i ;13
 SerialNRZ.5: v38.8o ;15
 SerialNRZ.6: v39.17i ;13
 SerialNRZ.6: v38.6o ;15
 SerialNRZ.7: v39.18i ;13
 SerialNRZ.7: v38.4o ;15
 SerialNRZ.8: v22.3i ;13
 SerialNRZ.8: #TP058.1i, v21.21o ;15
 SerialNRZ.8: v38.1i, v38.2i ;15
 SerialNRZ.9: v22.4i ;13
 SerialNRZ.9: v21.19o ;15
 Serviced: #TP050.1i, u45.3o ;14
 Serviced: u46.4i ;14
 ServiceTrap: u35.2i, u34.3i ;14
 ServiceTrap: u35.6o
 SetKReq': u68.6o, u98.3i ;14
 SetUp: u57.2o, u57.10i ;08
 SetUp: v25.6i ;08
 SetUp: u75.6i ;11
 Sk12: u93.6o, u93.12i ;23
 Sk16: u94.11o, u93.10i ;23
 Sk17: u93.8o, u93.13i ;23
 Sk1: u94.3o, u93.9i ;23
 Sk4: u94.5o, u93.5i ;23
 Sk8: u94.13i, u94.6o, u93.4i ;23
 SkCmpClk: u60.4o, u94.1i ;23
 SKY: u50.4i ;12
 SKY: u87.10i ;12
 SKY: v39.1i ;13
 SKY: v22.1i ;13
 SKY: u35.4i ;14
 SKY: u47.1i ;14
 SKY: u67.10i ;14
 SKY: u52.4i ;16
 SKY: u10.10i, u10.11i ;18
 SKY: u26.4i ;19
 SKY: u19.4i ;19
 SKY: u26.10i ;19
 SKY: u19.2i ;19
 SKY: u19.12i ;19
 SKY: u11.8i, u11.6i ;20

SKY: u11.5i ;20	SyncSA4Data: u08.9o ;21
SKY: u09.1i ;21	SyncSA4Data: u22.14i ;23
SKY: v00.2i ;21	
SKY: v00.13i ;21	SyncWdFound: u35.13i ;15
SKY: u09.10i ;21	SyncWdFound: u48.2i ;15
SKY: u08.13i ;21	SyncWdFound: u37.3i, u36.3i ;16
SKY: u08.10i ;21	SyncWdFound: #TP076.1i, u38.15o ;16
SKY: u39.4i ;22	SyncWdFound: u49.17i ;17
SKY: u08.4i ;22	
SKY: u08.2i ;22	SyncXferEnb: u39.1i, u24.1i ;22
SKY: u67.4i ;23	SyncXferEnb: u08.5o, #TP104.1i
SKY: u39.12i, u39.10i ;23	
SKY: u87.2i, u87.4i ;23	TA13: u28.3o ;02
SKY: #R1.2o ;24	TA13: u89.7i ;02
SKY: C230, C228 ;24	TA13: u91.6i ;11
SRefMFMClock: v00.5o, v00.12i ;21	TA1: u28.15o ;08
SrvcDet.0: u45.2i, u34.6o ;14	TA1: v23.11i ;08
SrvcDet.1: u45.1i, u34.5o, u34.7i ;14	TA1: v08.3i ;11
SServiced': u67.12o, u67.9i ;14	TA4: v09.14o ;08
SServiced: u67.8o ;14	TA4: v06.7i ;08
SServiced: u35.3i ;14	TA4: v08.4i ;11
SSrvcTrap: u34.2o, u34.4i ;14	TA5: v06.3o, v06.12i ;08
StartRead': u27.4o ;08	TA5: v23.6i ;08
StartRead': u92.12i ;08	TA5: v08.12o ;11
StartRead': u75.9o ;11	
Step': v05.15i ;13	TA6: v06.15o ;08
Step': u07.8o ;18	TA6: v23.3i ;08
Step': C236 ;24	TA6: v08.13o ;11
Step: v19.2o ;12	TB10: v09.15o ;08
Step: u07.9i ;18	TB10: v26.10i ;08
	TB10: u91.12o ;11
STransferEnable: u50.5o, u50.7i ;12	TB11: u27.1o ;08
SWriteCRC': #TP063.1i, u05.2o ;15	TB11: u76.4i ;08
SWriteCRC': u48.10i	TB11: u75.13o ;11
SWriteCRC: u66.2o ;14	TB1: u13.3o ;04
SWriteCRC: u59.2i ;15	TB1: u44.9o ;04
SWriteCRC: u05.1i ;15	TB1: v26.12i ;04
	TB1: v08.1i ;11
SyncClrDPReq': u98.12o, u82.10i ;04	TB5: u76.14o ;08
	TB5: v25.10i ;08
SyncClrKFlags': u66.1i, u98.9o ;14	TB5: v08.15o ;11
SyncClrKFlags': #TP057.1i	TB6: v26.13o ;08
SyncClrKFlags': u39.13i ;23	TB6: v06.10i ;08
SyncClrKFlags': u87.1i ;23	TB6: v08.2i ;11
SyncRcvMFM: u09.9o ;21	TB7: v26.5i ;08
SyncRcvMFM: u24.3i ;22	TB7: u57.14o ;08
	TB7: u91.10o ;11
	TB9: v26.2o, v26.6i ;08
	TB9: v08.14o ;11

TC1:	u30.9o	;04	TE2:	u58.2i	;11
TC1:	u44.11i	;04	TE3:	u56.14o	;04
TC1:	u73.13o	;04	TE3:	u30.12i	;04
TC1:	u29.9o	;11	TE3:	u43.15o	;11
TC2:	u30.15o	;04	Test1':	u83.1i	;02
TC2:	u73.14o	;04	Test1':	v42.1i	;03
TC2:	u44.10i	;04	Test1':	u80.1i	;03
TC2:	u29.2i	;11	Test1':	u77.1i	;03
TC3:	u27.12o	;08	Test1':	u96.1i	;07
TC3:	u92.11i	;08	Test1':	u95.1i	;07
TC3:	u91.11o	;11	Test1':	#TP114.1i, u64.11i	;10
TC5:	u57.3o, u57.13i	;08	Test1':	u65.13o	
TC5:	u58.13o	;11	Test1':	u35.1i	;14
TC6:	u30.2o	;08	Test1':	u19.10i	;19
TC6:	u57.11i	;08	Test1':	v00.4i, v00.10i	;21
TC6:	u58.5i	;11	Test1':	u09.4i	;21
TC7:	u76.2o	;08	Test1':	u09.13i	;21
TC7:	u57.5i	;08	Test1:	u64.10o	;10
TC7:	u43.3i	;11	Test1:	u06.2i, u06.12i	;23
TC9:	u27.13o	;04	Test2:	u76.9o	;02
TC9:	u30.7i	;04	Test2:	u74.12i, #TP003.1i	;02
TC9:	u29.10o	;11	Test2:	u75.5i	;11
TD11:	u28.13o, u28.11i	;08	Tick56':	u76.3o	;02
TD11:	u29.6i	;11	Tick56':	u28.4o	;02
TD12:	u28.14o, u28.12i	;08	Tick56':	v26.7i	;02
TD12:	u29.5i	;11	Tick56':	u75.10o	;11
TD1:	u30.3o	;04	Tick67':	v07.11i	;02
TD1:	u13.5i	;04	Tick67':	u89.10i	;02
TD1:	u29.1i	;11	Tick67':	v26.4o	;02
TD2:	u12.11i	;04	Tick67':	u91.7i	;11
TD2:	u13.14o	;04	TimingClock:	u06.11o, u22.6i	;23
TD2:	u29.3i	;11	Tick7':	u74.5i, u74.4o	;02
TD3:	u12.14i	;04	Tick7':	u30.6i	;04
TD3:	u44.12i	;04	Tick7':	u30.4i	;08
TD3:	u13.15o	;04	Tick7':	u92.13i	;08
TD3:	u43.12o	;11	Tick7':	u58.15o	;11
TD4:	u13.2o	;04	Track00:	v02.13i	;13
TD4:	u44.13i	;04	Track00:	u05.8o	;20
TD4:	u43.14o	;11	TstAddrMkPrm':	u65.6i, #TP116.1i	;27
TD7:	v26.14o	;08	TstAddrMkPrm':	u51.9i	
TD7:	u12.2i	;08	TstAddrMkPrm:	u25.10i, u23.10i	;22
TD7:	u43.2i	;11	TstAddrMkPrm:	u23.8i, u25.8i	
TE2:	u42.14o	;04	TstAddrMkPrm:	u51.8o	;27
TE2:	u56.5i	;04			

TstDataBorder': u65.1i, #TP111.1i ;10
 TstDataBorder': u64.1i
 TTLDB.3: v14.12o, v01.9o ;05
 TTLDB.3: #TP023.1i, v16.9o
 TTLDB.3: v15.12o, u55.11i
 TTLDB.4: v14.11o, v01.12o ;05
 TTLDB.4: #TP024.1i, v16.12o
 TTLDB.4: v15.11o, u41.5i
 TTLDB.5: v12.15o, v01.15o ;05
 TTLDB.5: #TP025.1i, v16.15o
 TTLDB.5: v11.15o, u41.7i
 TTLDB.6: v12.14o, v01.16o ;05
 TTLDB.6: #TP026.1i, v16.16o
 TTLDB.6: v11.14o, u41.10i
 TTLDB.7: v12.13o, v01.19o ;05
 TTLDB.7: #TP027.1i, v16.19o
 TTLDB.7: v11.13o, u41.11i
 TTLLastTick: u69.12i ;07
 TTLLastTick: u12.4o ;08
 TTLVideo': u15.5o ;10
 TTLVideo': v05.17i ;13
 TTLVideo: u15.4o ;10
 TTLVideo: v05.2i ;13
 TwoBit: u74.2o ;02
 TwoBit: u28.7i ;02
 TwoBit: u58.1i ;11
 UnCompMFM: u01.1i ;17
 UnCompMFM: u31.15o ;17
 UnLdCtlFifo: v32.16i, v13.16i ;06
 UnLdCtlFifo: v27.16i, v31.16i
 UnLdCtlFifo: u69.11o ;07
 UWriteEnable': u02.1i ;18
 UWriteEnable': u60.12i, u60.10o ;21
 UWriteEnable': u60.11i
 UWriteEnable: u10.7i, u10.6i ;18
 UWriteEnable: #TP090.1i, u60.13o ;21
 UWriteEnable: u21.1i
 Vbb: v24.11i, v24.6i, v24.14i ;02
 Vbb: v24.2i, v24.1i
 Vbbc18: v23.1i, v23.10i, v23.14i ;08
 Vbbc18: v23.2i, v23.7i
 Vbbf13: u12.10i, u12.15i, u12.7i ;04
 Vbbf13: u12.1i, u12.3i ;08
 Vbbg7: u15.6i, u15.2i, u15.1i ;10

VCC: #C93.1o, #TP001.1i, #F2.1o ;01
 VCC: v24.9i ;02
 VCC: u73.9i ;02
 VCC: u41.9i ;05
 VCC: u55.9i ;05
 VCC: u27.9i ;08
 VCC: v23.9i ;08
 VCC: u12.9i ;08
 VCC: #R34.2o ;09
 VCC: u15.9i ;10
 VCC: #R1.1i ;24
 VCC: #L4.1o ;25
 VCC: #CR3.1o ;26
 VCC: #R12.1o ;26
 VCC: #R13.1o ;26
 VCC: #C24.1o, #R25.2i ;26
 VCC: u40.7i ;26
 VCC: #C46.1i, #C47.1i, #C48.1i ;28
 VCC: #C49.1i, #C50.1i, #C51.1i
 VCC: #C52.1i, #C56.1i, #C57.1i
 VCC: #C58.1i, #C59.1i, #C60.1i
 VCC: #C63.1i, #C64.1i, #C65.1i
 VCC: #C66.1i, #C67.1i, #C68.1i
 VCC: #C69.1i, #C4.1i, #C5.1i
 VCC: #C6.1i, #C7.1i, #C8.1i
 VCC: #C9.1i, #C12.1i, #C13.1i
 VCC: #C14.1i, #C15.1i, #C16.1i
 VCC: #C17.1i, #C18.1i, #C36.1i
 VCC: #C37.1i, #C38.1i, #C39.1i
 VCC: #C70.1i, #C73.1i, #C74.1i
 VCC: #C75.1i, #C76.1i, #C77.1i
 VCC: #C79.1i, #C80.1i, #C81.1i
 VCC: #C82.1i, #C83.1i, #C84.1i
 VCC: #C85.1i, #C86.1i, #C87.1i
 VCC: #C88.1i, #C89.1i, #C90.1i
 VCC: #C91.1i

 VEE: #C92.2o, #TP002.1i, #F1.1o ;01
 VEE: C8 ;09
 VEE: #R7.2i ;09
 VEE: #R8.2i ;09
 VEE: u43.8i, u75.8i, u91.8i ;09
 VEE: v08.8i, u29.8i
 VEE: u11.13i ;20
 VEE: #R6.1i, #C42.2i ;25
 VEE: #R35.2i ;25
 VEE: #CR4.2i ;26
 VEE: #C25.1o, #R28.2i ;26
 VEE: u40.4i ;26
 VEE: #C1.1i, #C10.1i, #C11.1i ;28
 VEE: #C20.1i, #C21.1i, #C22.1i
 VEE: #C33.1i, #C34.1i, #C35.1i
 VEE: #C44.1i, #C45.1i, #C53.1i
 VEE: #C54.1i, #C55.1i, #C61.1i
 VEE: #C62.1i, #C71.1i, #C72.1i
 VEE: #C78.1i

 VerifyError: v04.11i ;13

VerifyError: u66.5o ;14
 Vert': u83.8o ;04
 Vert': u82.4i ;04

 Vert: u83.9o ;04
 Vert: u88.5i ;04

 VertClk: u81.12o ;04
 VertClk: u83.11i ;04

 Video': u14.2o ;04
 Video': #CR1.2i, #R7.1o, C6 ;09
 Video': u15.7i ;10

 Video: u14.3o ;04
 Video: #CR2.2i, #R8.1o, C5 ;09
 Video: u15.3i ;10

 VSync': #R10.1o, #L2.1o, C3 ;09

 Wait: E17, v46.9i ;03

 WakeupControl.0: v19.15o ;12
 WakeupControl.0: u68.10i ;14

 WakeupControl.1: #TP047.1i ;12
 WakeupControl.1: v19.16o
 WakeupControl.1: u68.11i ;14
 WakeupControl.1: u46.7i ;14
 WakeupControl.1: u37.7i, u36.7i ;16

 WC.0: #TP037.1i, u61.12o, u62.3i ;07

 WC.1: #TP038.1i, u61.13o, u62.4i ;07

 WC.2: #TP039.1i, u61.14o, u62.7i ;07

 WordBoundary': v44.11i, v40.11i ;13
 WordBoundary': u66.11i ;14
 WordBoundary': u52.5o ;16

 WPulse': u88.8o, u81.11i ;04

 WPulse: v24.5o, E7 ;02
 WPulse: u88.9i ;04

 WrDatClk: v20.11i, u86.6o, v37.11i ;12

 WriteCRC: v19.12o ;12
 WriteCRC: u66.3i ;14

 WriteData.0: v37.2o ;12
 WriteData.0: v38.22i ;15

 WriteData.10: v20.6o ;12
 WriteData.10: v21.18i ;15

 WriteData.11: v20.9o ;12

WriteData.11: v21.16i ;15	X.0: v02.18o ;13
WriteData.12: v20.12o ;12	X.10: E46, v18.6i ;10
WriteData.12: v21.9i ;15	X.10: v05.14o ;13
WriteData.13: v20.15o ;12	X.10: v40.6o ;13
WriteData.13: v21.7i ;15	X.10: v04.14o ;13
WriteData.14: v20.16o ;12	X.11: E146, v18.8i ;10
WriteData.14: v21.5i ;15	X.11: v05.12o ;13
WriteData.15: v20.19o ;12	X.11: v40.9o ;13
WriteData.15: v21.3i ;15	X.11: v04.12o ;13
WriteData.1: v37.5o ;12	X.12: E47, v18.17i ;10
WriteData.1: v38.20i ;15	X.12: v05.3o ;13
WriteData.2: v37.6o ;12	X.12: v40.12o ;13
WriteData.2: v38.18i ;15	X.12: v04.3o ;13
WriteData.3: v37.9o ;12	X.13: E147, v18.15i ;10
WriteData.3: v38.16i ;15	X.13: v05.5o ;13
WriteData.4: v37.12o ;12	X.13: v40.15o ;13
WriteData.4: v38.9i ;15	X.13: v04.5o ;13
WriteData.5: v37.15o ;12	X.14: E48, v18.13i ;10
WriteData.5: v38.7i ;15	X.14: v05.7o ;13
WriteData.6: v37.16o ;12	X.14: v40.16o ;13
WriteData.6: v38.5i ;15	X.14: v04.7o ;13
WriteData.7: v37.19o ;12	X.15: E148, v18.11i ;10
WriteData.7: v38.3i ;15	X.15: v05.9o ;13
WriteData.8: v20.2o ;12	X.15: v40.19o ;13
WriteData.8: v21.22i ;15	X.15: v04.9o ;13
WriteData.9: v20.5o ;12	X.1: E141, v35.4i ;10
WriteData.9: v21.20i ;15	X.1: v03.16o ;13
WriteData.9: v21.20i ;15	X.1: v44.5o ;13
WriteData.9: v21.20i ;15	X.1: v02.16o ;13
WriteEnable': u05.12o, u03.11i ;12	X.2: E42, v35.6i ;10
WriteEnable: u05.13i, v19.19o ;12	X.2: v03.14o ;13
WriteEnable: u05.13i, v19.19o ;12	X.2: v44.6o ;13
WriteEnable: u05.13i, v19.19o ;12	X.2: v02.14o ;13
WriteFault': u20.5i ;20	X.3: E142, v35.8i ;10
WriteFault': u18.5i ;20	X.3: v03.12o ;13
WriteFault': C244 ;24	X.3: v44.9o ;13
WriteFault': C244 ;24	X.3: v02.12o ;13
WriteFault: v04.17i ;13	X.4: E43, v35.17i ;10
WriteFault: u20.6o ;20	X.4: v03.3o ;13
WriteFault: u20.6o ;20	X.4: v44.12o ;13
WriteFault: u20.6o ;20	X.4: v02.3o ;13
WriteGate': v05.11i ;13	X.5: E143, v35.15i ;10
WriteGate': u02.6o ;18	X.5: v03.5o ;13
WriteGate': C240 ;24	X.5: v44.15o ;13
WriteGate': C240 ;24	X.5: v02.5o ;13
X.0: E41, v35.2i ;10	X.6: E44, v35.13i ;10
X.0: v44.2o ;13	X.6: v03.7o ;13
X.0: v03.18o ;13	X.6: v03.7o ;13

X.6:	v44.16o ;13	Y.14:	v16.17i ;05
X.6:	v02.7o ;13	Y.14:	E58, v33.17i ;06
X.7:	E144, v35.11i ;10	Y.15:	v16.18i ;05
X.7:	v03.9o ;13	Y.15:	E158, v33.18i ;06
X.7:	v44.19o ;13	←KIData': v40.1i, E32, v44.1i ;13	
X.7:	v02.9o ;13	←KIData': u67.1i ;14	
X.8:	E45, v18.2i ;10	←KStatus': v04.1i, v02.19i, v02.1i ;13	
X.8:	v05.18o ;13	←KStatus': E132, v04.19i	
X.8:	v40.2o ;13	←KTest': v05.1i, v03.19i, v03.1i ;13	
X.8:	v04.18o ;13	←KTest': E33, v05.19i	
X.9:	E145, v18.4i ;10		
X.9:	v05.16o ;13		
X.9:	v40.5o ;13		
X.9:	v04.16o ;13		
Y.00:	v01.3i ;05		
Y.00:	E49, v34.3i ;06		
Y.01:	v01.4i ;05		
Y.01:	E149, v34.4i ;06		
Y.02:	v01.7i ;05		
Y.02:	E52, v34.7i ;06		
Y.03:	v01.8i ;05		
Y.03:	E152, v34.8i ;06		
Y.04:	v01.13i ;05		
Y.04:	E53, v34.13i ;06		
Y.05:	v01.14i ;05		
Y.05:	E153, v34.14i ;06		
Y.06:	v01.17i ;05		
Y.06:	E54, v34.17i ;06		
Y.07:	v01.18i ;05		
Y.07:	E154, v34.18i ;06		
Y.08:	v16.3i ;05		
Y.08:	E55, v33.3i ;06		
Y.09:	v16.4i ;05		
Y.09:	E155, v33.4i ;06		
Y.10:	v16.7i ;05		
Y.10:	E56, v33.7i ;06		
Y.11:	v16.8i ;05		
Y.11:	E156, v33.8i ;06		
Y.12:	v16.13i ;05		
Y.12:	E57, v33.13i ;06		
Y.13:	v16.14i ;05		
Y.13:	E157, v33.14i ;06		